Title: PCIe Memory
Students: ECE, ECE, ECE
Topics: FPGA Design, Microcontroller Coding, Design, PCB Design, Communication Protocols, PC Driver Programming

Description
As you may be aware from our most recent processor announcements, we have changed our CPU architecture to integrate the memory controller as one unit. This presents a potential problem at first power on and early debugging – if the integrated memory is not functional, very little debugging can be done. So we would like an add-in card with enough memory to boot an OS (e.g., windows). The current suggestion is to use one of the PCIe endpoint devices to interface to common memory DIMM. The endpoint devices are readily available. A common memory DIMM such as DDR2 could be selected. There are many FPGA devices that could be used to interface between the endpoint and the DIMM. Several of the FPGA vendors have DDR2 memory controller solutions. This is the basic need.

Absolute Minimum Requirements
• Interface memory module to PCIe bus
• Systems to prevent damage to PC
• Mentor to sign off on design prior to fabrication

Desired Features
• Incorporates LAN or USB port
• Have SM (System Management) Bus/I²C bus
• MCU can be reset to SM Bus