Lecture 14: Sequential Blocks

Matthew Shuman
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1 Registers — 6-1 in Text

Connecting D flip flops in parallel, as shown in figure 1, creates a register. A simulation of the circuit in figure 1 creates figure 2. The key point to take away from the simulation is that a rising edge of the register clock causes the input to be copied into the register outputs.

Figure 1: 4 flip flops in parallel create a 4 bit register

Figure 2: This simulation shows how a four bit register operates.
2 Registers — 6-2 in Text

Connecting D flip flops in series creates a shift register. The block symbol for a shift register is shown in figure 3. A simulation of the circuit in figure 3 creates figure 4. The key point to take away from the simulation is that a rising edge of the register clock causes SLI to be loaded into the LSB, shifting all of the register contents to the left.

Figure 3: 4 D flip flops in series create a 4 bit shift register

Figure 4: This simulation shows how a four bit shift register operates.

3 Counters — 6-3 in Text

A commonly used state machine is a counter. Counters are useful in generating signals for a NES controller, a PWM signal for a motor, or control signals for a servo. Figure 5 shows an example block for a premade counter. A simulation of the circuit in figure 5 creates figure 6. The key point to take away from the simulation is that a rising edge of the counter clock the output to increment by one.
Figure 5: This counter has several controlling inputs.

Figure 6: This simulation shows how a four bit counter operates.