Homework 6
Matthew Shuman
Due November 12th, 2010

Problems are from the ECE 271 textbook.

Structural Modeling in Verilog

1. Draw the structural diagram for the NES_Reader
   Include the follow items:
   All module names
   All instance names
   All input/output port names
   All net names

Sequential Logic in Verilog

2. 4.22
3. 4.23
4. 4.44

Interview Questions

5. Problem 4.1 in the text.

Extra Credit

For one point each:

1. Draw the hardware inside of the four_bit_counter module used in problem 1.
2. Draw the hardware inside of the nes_clock_state_decoder module used in problem 1.
3. Draw the hardware inside of the nesLatch_state_decoder module used in problem 1.
4. Draw the hardware inside of the nes_data_receiver_decoder module used in problem 1.

1http://classes.engr.oregonstate.edu/eecs/fall2010/ece271/VerilogExamples/NES/nes_reader.v