ECE442
SENIOR DESIGN PROJECT

Term: Fall 2010 / Winter 2011 / Spring 2011
Text: Design for Electrical and Computer Engineers
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Course Overview

ECE441/2/3 is the Electrical Engineering capstone design sequence. This three-course sequence provides practical experience in new product development and project management through the design, manufacturing, and testing of a new product or process. Course topics include Project Planning and Scheduling, Marketing and Quality Functional Deployment, and Product Development. Specifically the sequence consists of creating a paper describing the complete design by the end of ECE441, construction of a prototype (including design iteration) during ECE442, and presentation of the completed refined and tested project in ECE443. The sequence must be taken in consecutive terms. While attendance of organizational lectures and seminars is mandatory, the majority of the work in this sequence occurs outside of class. Students should expect to spend approximately 240 hours of total time on the project per student.

As well as being the department’s capstone sequence, ECE441/2/3 is also Electrical Engineering’s designated writing-intensive (WIC) sequence. As such, students enrolled in this sequence complete a variety of formal written and oral assignments that support the design process and further their engineering communications skills. In completing these assignments, ECE441/2/3 students are expected to review and respond to one another’s writing, revise individually and collaboratively produced drafts and use informal writing techniques to explore and solve engineering design problems.

It is important to remember that success in this course is your responsibility. Do not depend on the faculty advisor, sponsor, or mentor to keep your project on schedule. Advisors and mentors will support and guide you in completing your project successfully, but you must take the initiative and seek out their help. A successful project is worth your effort and provides a tangible example of your capabilities to potential employers.

Course Learning Outcomes

At the completion of the courses, students will be able to perform the following tasks:
1. Plan, schedule, and carry out an engineering design project.
2. Develop and implement an electrical system using effective design/project techniques.
3. Design and implement test plans and evaluate results.
4. Collaboratively produce written project reports that effectively communicate project information to their target audience(s)—i.e., that are rhetorically appropriate for these audiences and follow disciplinary conventions of usage, vocabulary, format, and citation.
5. Participate effectively in the peer review process.
6. Compose a variety of job-search-related texts, including resumes, cover letters, and professional email communications.
7. Prepare and present formal project-management reviews and other oral presentations.

ABET Outcomes

1. Write a concise project description stemming from an identified objective. (ABET outcomes e, f, g)
2. Collect and review technical information on a project from relevant external resources. (ABET outcomes e, j)
3. Project the impact constraints for projects (Resources, Time, Finances) (ABET outcomes d, f)
4. Record technical results and measure progress. (ABET outcomes d, g)
5. Acquire tooling and hardware (components) for a breadboard / prototype. (ABET outcome k)
6. Present project information succinctly to a technically aware audience. (ABET outcomes a, f, g)
Academic Dishonesty

At Oregon State University academic dishonesty is defined by the Oregon Administrative Rules 576-015-0020.1.a-c as: An intentional act of deception in which a student seeks to claim credit for the work or effort of another person or uses unauthorized materials or fabricated information in any academic work.

Academic dishonesty includes:

- **CHEATING** - use or attempted use of unauthorized materials, information or study aids or an act of deceit by which a student attempts to misrepresent mastery of academic effort or information. This includes unauthorized copying or collaboration on a test or assignment or using prohibited materials and texts.

- **FABRICATION** - falsification or invention of any information (including falsifying research, inventing or exaggerating data and listing incorrect or fictitious references).

- **ASSISTING** - helping another commit an act of academic dishonesty. This includes paying or bribing someone to acquire a test or assignment, changing someone's grades or academic records, or taking a test/doing an assignment for someone else (or allowing someone to do these things for you). It is a violation of Oregon state law to create and offer to sell part or all of an education assignment to another person (ORS 165.114).

- **TAMPERING** - altering or interfering with evaluation instruments and documents.

- **PLAGIARISM** - representing the word or ideas of another person as one's own OR presenting someone else's words, ideas, artistry or data as one's own. This includes copying another person's work (including unpublished material) without appropriate referencing, presenting someone else's opinions and theories as one's own, or working jointly on a project, then submitting it as one's own.

IEEE Code of Ethics

As a community of Electrical and Computer Engineers, we have a duty to present ourselves and our profession to each other and the public in the best light possible. The IEEE has a code of Ethics that should always be considered. It reads:

“We, the members of the IEEE, in recognition of the importance of our technologies in affecting the quality of life throughout the world, and in accepting a personal obligation to our profession, its members and the communities we serve, do hereby commit ourselves to the highest ethical and professional conduct and agree:

1. to accept responsibility in making decisions consistent with the safety, health and welfare of the public, and to disclose promptly factors that might endanger the public or the environment;
2. to avoid real or perceived conflicts of interest whenever possible, and to disclose them to affected parties when they do exist;
3. to be honest and realistic in stating claims or estimates based on available data;
4. to reject bribery in all its forms;
5. to improve the understanding of technology, its appropriate application, and potential consequences;
6. to maintain and improve our technical competence and to undertake technological tasks for others only if qualified by training or experience, or after full disclosure of pertinent limitations;
7. to seek, accept, and offer honest criticism of technical work, to acknowledge and correct errors, and to credit properly the contributions of others;
8. to treat fairly all persons regardless of such factors as race, religion, gender, disability, age, or national origin;
9. to avoid injuring others, their property, reputation, or employment by false or malicious action;
10. to assist colleagues and co-workers in their professional development and to support them in following this code of ethics.”
MAJOR ASSIGNMENTS AND PERCENT OF COURSE GRADE

LATE WORK POLICY
All late work will receive no credit. Only pre-discussed exceptions will be accepted.

BIWEEKLY MEETINGS (200 POINTS) – INDIVIDUAL GRADE
Submitted during special time
During weeks 12, 14, 16, and 18 of the term, each group will meet with a member of the senior design staff. The meeting will be 30 minutes in length. Prior to the meeting, student groups should have posted at least 5 new tickets per person to Beaversource. During the meeting, previous tasks will be reviewed and newly created tasks reviewed. These points are individually assigned.

The week 20 meeting will be your opportunity to present your final system for grading according to the Final Project review assignment.

MIDTERM PROJECT REVIEW (220 POINTS) – GROUP/INDIVIDUAL GRADE
The midterm project review is conducted with your team members and one or more members of the ECE senior design instructional team. You will be reviewed on your personal and group progress on the project. By the midterm review your group should have completed designing and building every block in your design including testing and Beaversource must be updated. The blocks should be assembled into a system but the system tests may not be successful. Electronic copies of all important datasheets must be on BeaverSource before the review time. They should be linked from each block that uses the datasheet. Datasheets for each silicon or electro-mechanical part must be included. Any ‘special’ components not covered by this statement must also have datasheets included. Additionally, evidence of each block passing its required test must present on Beaversource.

Each group will be expected to meet during the same time as they would meet with TAs for Biweekly meetings. All of the meeting will be in DB211. Please come ready to demonstrate any block tests noted as successful on Beaversource.

MIDTERM PEER REVIEW (100 POINTS) - INDIVIDUAL GRADE
Copies to Instructor (TEACH Submission)
All group members will individually prepare a “peer review,” which will uploaded to TEACH individually. In these reviews, students will reflect on their own work and their peers work. Specific topics to be addressed in this evaluation will be provided. Due Monday by 5PM of Week 15.

FINAL PROJECT REVIEW (400 POINTS). – GROUP
The final project review is to be held during week 20 of the term. Electronic copies of all important datasheets must be on Beaversource before the scheduled review. They should be linked from each block that uses the datasheet. Datasheets for each silicon or electro-mechanical part must be included. Any ‘special’ components not covered by this statement must also have datasheets included. Additionally all of your testing should be updated with proof added.

During the Biweekly meeting time in week 20, each group will demonstrate their project. Some groups may require more time and will be arranged on an individual basis. During this time, you will show your design, and be asked questions about its operation. You should be prepared to show any of the system tests that you have reported as completed. Your score it based on if your design meets all of the engineering requirements developed in Fall term.

FINAL PEER REVIEW (80 POINTS) - INDIVIDUAL GRADE
Copies to Instructor (hard copy)
All group members will individually prepare a “peer review,” which will need to be printed and slipped under mt door in KEC1117. In these reviews, students will reflect on their own work and their peers work. Specific topics to be addressed in this evaluation will be provided. The form provided online MUST be used to receive credit. Due Monday by 5PM of Finals week

EXTRA CREDIT (??? Points) – INDIVIDUAL GRADING
Throughout the term, you will be given opportunities to earn extra credit by attending extra lectures and seminars. Based on the content and length of the seminar, a varying amount of extra credit will be given.
Watch the Google calendar for these opportunities. Be sure to fill out the sign-up sheet at these events.

COURSE SCHEDULE
The course schedule and details of each lecture is available on the ‘Google™ calendar.’ While no changes are expected, please review it periodically to double check.

**IMPORTANT INFORMATION**

**BUDGET**
Each group will have access to a budget of $200 starting in November. Projects that need more finding will be able to request more during the month of December. Make intelligent choices when defining your required components. There are multiple opportunities for free/or sample parts, but beware: YOU GET WHAT YOU PAY FOR. If you need parts from the vendors below, follow the steps to get parts:

**Analog Devices**
- Go to the link below and fill out the form.
- [https://form.analog.com/Form_Pages/corporate/parts.aspx](https://form.analog.com/Form_Pages/corporate/parts.aspx)

**National Semiconductor**
- Go to the link below.
- Find your part.
- If there is a sample button, send the part number to Donald Heer.
- If there is not a sample button, the part cannot be sampled.

**Texas Instruments**
- Enter the TI Analog University Design Contest at the link below. Follow the steps to sample parts.

**BEAVERSOURCE**
BeaverSource is a university sponsored tool for project management. At a minimum you will use BeaverSource to organize and display your design specification. You are encouraged however to fully utilize the abilities of the tool since it is likely to make you life easier. Some important things you could look into are the SVN abilities for software, and more advanced use of the ticketing/bug tracking systems.

**DB211 Lab Policies**

**Clean-up:**
As needed, the graduate TAs will come by the lab at 1pm on Mondays to clean up the lab. Any materials left on a desk not currently occupied will be gently placed into a large box and left near the main door. Exempt items include laptops and appliances. Loose chips and the like will not be spared.

**Be Considerate:**
We all need to share the room. Please be considerate. Use headphones and shower as to avoid interpersonal conflicts. Do not leave your materials spread all over even if ‘you are only leaving for a few hours’ as the space maybe needed by another group.

**Tools and Safety:**
A small first aid kit will be attached to the wall near the entry door in the upcoming days. Please only use this kit as needed. Be aware of the tools you are using and turn them off prior to leaving the lab. The tools are a shared resource, if all of the soldering iron tips become damaged due to long term heating, it hurts everyone.