3.1
\[ S \quad R \quad Q \quad XXX \quad XXX \quad \text{Unknown Value} \]

3.2
\[ CLK \quad D \quad Q \quad XXX \]

3.4 This is sequential logic. If \( \overline{S} \) and \( \overline{R} \) are both high, the outputs don't change. If \( S \) goes low, Q goes high which makes \( \overline{Q} \) go low. If \( R \) goes low, \( \overline{Q} \) goes high which makes Q go low. If both \( S \) and \( R \) go low this is an active low \( \overline{S} \overline{R} \) latch.

3.7 a) \[ \begin{array}{cc}
\overline{S} & \overline{R} \\
00 & 00 \\
00 & 01 \\
01 & 10 \\
10 & 10 \\
11 & 11 \\
\end{array} \quad \begin{array}{cc}
D^* & 0 \\
0 & 1 \\
0 & 0 \\
1 & 0 \\
0 & 1 \\
1 & 0 \\
\end{array} \]

\[ D^* = \overline{S} \overline{K} \overline{Q} + \overline{S} \overline{K} + \overline{S} K \overline{Q} \]

b) \[ \begin{array}{cc}
D & \overline{S} \\
0 & 0 \\
0 & 1 \\
1 & 0 \\
1 & 1 \\
\end{array} \quad \begin{array}{cc}
D^* & 0 \\
0 & 1 \\
0 & 0 \\
1 & 0 \\
1 & 1 \\
\end{array} \]

c) \[ \begin{array}{cc}
V_{CC} & \overline{S} \\
0 & 0 \\
0 & 1 \\
1 & 0 \\
1 & 1 \\
\end{array} \quad \begin{array}{cc}
D^* & 0 \\
0 & 1 \\
0 & 0 \\
1 & 0 \\
1 & 1 \\
\end{array} \]
3.12

3.13  
\[ \text{Frequency Range} = \frac{1}{2N \cdot T_{pd}} \text{ to } \frac{1}{2N \cdot T_{pd}} \]

3.19  See Lecture #7 notes

I.4 3.3  
A latch updates the output whenever the enable is high. It is level driven.

A flip-flop updates the output during a rising or falling edge. It is edge driven.