COURSE OVERVIEW

ECE441/2/3 is the Electrical Engineering capstone design sequence. The course is intended to follow the engineering design model shown. The cycle is divided out over the various terms with the intention of a finished fully tested project being ready for the engineering expo. Research projects are also possible using the same model.

During ECE441, we will be describing the system level architecture. Once the top-level design is completed, we will continue to design the sub-blocks based on our specifications. While it will not be required, some basic implementation of the individual blocks is suggested as it will help create the design.

In ECE442, we will finish the implementation of the sub-blocks and after each one has been implemented and validated it will be integrated into the system level. Complete validation will not be needed until ECE443, but some of the system requirements will need to be validated during ECE442.

Finally in ECE443, we will finish out the project passing all system validation tests and presenting projects at the Engineering Expo.

It is important to remember that success in this course is your responsibility. Do not depend on the faculty advisor, sponsor, or mentor to keep your project on schedule. Advisors and mentors will support and guide you in completing your project successfully, but you must take the initiative and seek out their help. A successful project is worth your effort and provides a tangible example of your capabilities to potential employers.

COURSE LEARNING OUTCOMES

At the completion of the courses, students will be able to perform the following tasks:

1. Plan, schedule, and carry out an engineering design project.
2. Develop and implement an electrical system using effective design/project techniques.
3. Design and implement test plans and evaluate results.
4. Collaboratively produce written project reports that effectively communicate project information to their target audience(s)—i.e., that are rhetorically appropriate for these audiences and follow disciplinary conventions of usage, vocabulary, format, and citation.
5. Participate effectively in the peer review process.
6. Compose a variety of job-search-related texts, including resumes, cover letters, and professional email communications.
7. Prepare and present formal project-management reviews and other oral presentations.

ABET OUTCOMES
1. Write a concise project description stemming from an identified objective. (ABET outcomes e, f, g)
2. Collect and review technical information on a project from relevant external resources. (ABET outcomes e, j)
3. Project the impact constraints for projects (Resources, Time, Finances) (ABET outcomes d, f)
4. Record technical results and measure progress. (ABET outcomes d, g)
5. Acquire tooling and hardware (components) for a breadboard / prototype. (ABET outcome k)
6. Present project information succinctly to a technically aware audience. (ABET outcomes a, f, g)

WIC Requirements:
7. Develop and articulate content knowledge and critical thinking in the discipline through frequent practice of informal and formal writing.
8. Demonstrate knowledge/understanding of audience expectations, genres, and conventions appropriate to communicating in the discipline.
9. Demonstrate the ability to compose a document of at least 2000 words through multiple aspects of writing, including brainstorming, drafting, using sources appropriately, and revising comprehensively after receiving feedback on a draft.
Academic Dishonesty

At Oregon State University academic dishonesty is defined by the Oregon Administrative Rules 576-015-0020.1.a-c as: An intentional act of deception in which a student seeks to claim credit for the work or effort of another person or uses unauthorized materials or fabricated information in any academic work.

Academic dishonesty includes:

- **CHEATING** - use or attempted use of unauthorized materials, information or study aids or an act of deceit by which a student attempts to misrepresent mastery of academic effort or information. This includes unauthorized copying or collaboration on a test or assignment or using prohibited materials and texts.

- **FABRICATION** - falsification or invention of any information (including falsifying research, inventing or exaggerating data and listing incorrect or fictitious references.

- **ASSISTING** - helping another commit an act of academic dishonesty. This includes paying or bribing someone to acquire a test or assignment, changing someone's grades or academic records, or taking a test/doing an assignment for someone else (or allowing someone to do these things for you). It is a violation of Oregon state law to create and offer to sell part or all of an education assignment to another person (ORS 165.114).

- **TAMPERING** - altering or interfering with evaluation instruments and documents.

- **PLAGIARISM** - representing the word or ideas of another person as one's own OR presenting someone else's words, ideas, artistry or data as one's own. This includes copying another person's work (including unpublished material) without appropriate referencing, presenting someone else's opinions and theories as one's own, or working jointly on a project, then submitting it as one's own.

IEEE Code of Ethics

As a community of Electrical and Computer Engineers, we have a duty to present ourselves and our profession to each other and the public in the best light possible. The IEEE has a code of Ethics that should always be considered. It reads:

“We, the members of the IEEE, in recognition of the importance of our technologies in affecting the quality of life throughout the world, and in accepting a personal obligation to our profession, its members and the communities we serve, do hereby commit ourselves to the highest ethical and professional conduct and agree:

1. to accept responsibility in making decisions consistent with the safety, health and welfare of the public, and to disclose promptly factors that might endanger the public or the environment;
2. to avoid real or perceived conflicts of interest whenever possible, and to disclose them to affected parties when they do exist;
3. to be honest and realistic in stating claims or estimates based on available data;
4. to reject bribery in all its forms;
5. to improve the understanding of technology, its appropriate application, and potential consequences;
6. to maintain and improve our technical competence and to undertake technological tasks for others only if qualified by training or experience, or after full disclosure of pertinent limitations;
7. to seek, accept, and offer honest criticism of technical work, to acknowledge and correct errors, and to credit properly the contributions of others;
8. to treat fairly all persons regardless of such factors as race, religion, gender, disability, age, or national origin;
9. to avoid injuring others, their property, reputation, or employment by false or malicious action;
10. to assist colleagues and co-workers in their professional development and to support them in following this code of ethics.”
MAJOR ASSIGNMENTS AND PERCENT OF COURSE GRADE

LATE WORK POLICY
All late work will receive no credit. Only pre-discussed exceptions will be accepted.

PEER REVIEW REFLECTION (50 Points) – INDIVIDUAL GRADING
Printed copies to Instructor (KEC1148) AND PDF submission to TEACH
By the beginning of week 12, each student will have reviewed and reflected on the peers reviews from the end of the previous term. Based on these reflections, each student will list a few things they will attempt in order to correct the problems observed. This reflection will be turned into the course instructor and a copy given to each group mate. This is due on 4PM on Monday of week 12.

1:1 MEETINGS (50 POINTS) – INDIVIDUAL GRADING
Each student is required to attend a 1:1 meeting with the course instructor. Sign-ups are done via the Google™ Calendar link. Points are assigned based on student preparedness and promptness.

SYSTEM TESTING UPDATES (100 POINTS) – GROUP GRADE
4PM on Monday of Week 14.
Each group is responsible for reviewing and updating their system tests (Section 2 of Beaversource). These updates should ensure that each test meets the criteria of the course textbook (Section 7). The group should then print out Section 2 and the sign-off sheet. Sign the sign-off sheet and submit the entire package as a PDF to TEACH by 4pm on Monday of Week 14.

BI-WEEKLY SCRUM MEETINGS (150 POINTS) – INDIVIDUAL GRADING
Submitted during special time
Starting week 2 of the term, each group will meet with the teaching assistants during a special time every other week. The meeting will be 30-45 minutes in length. These meetings will be based on the SCRUM model and will cover what happened in the previous sprint, examine any new customer stories, and define what will be accomplished over the next sprint. The TA does not assign the scores per student. These points are assigned by course instructor.

MIDTERM PROJECT REVIEW (350 POINTS) – INDIVIDUAL GRADE
The midterm project review is conducted with your team members and one or more members of the ECE senior design instructional team. You will be reviewed on your personal and group progress on the project. By the midterm review each individual should have completed designing and building the blocks in your design they are responsible for. To receive credit, the corresponding Beaversource section must be updated. Electronic copies of all important datasheets must be on BeaverSource before the review time. They should be linked from each block that uses the datasheet. Datasheets for each silicon or electro-mechanical part must be included. Any ‘special’ components not covered by this statement must also have datasheets included. Additionally, evidence of each block passing its required test must present on Beaversource page for that block.

Each group will be expected to meet during a specially chosen time. All of the meetings will be in DB211. Please come ready to demonstrate any block tests noted as successful on Beaversource.

FINAL PROJECT REVIEW (250 POINTS) – GROUP
The final project review is to be held during week 20 of the term. Electronic copies of all important datasheets must be on Beaversource before the scheduled review. They should be linked from each block that uses the datasheet. Datasheets for each silicon or electro-mechanical part must be included. Any ‘special’ components not covered by this statement must also have datasheets included. Additionally to get credit for a passed test, there must be proof of that test in the Testing section (section 5) of your Beaversource page.

During a special meeting time in week 20, each group will demonstrate their project. Some groups may require more time and will be arranged on an individual basis. During this time, you will show your design, and be asked questions about its operation. You should be prepared to show any of the system tests that you have reported as completed. Your score is based on if your design meets all of the engineering requirements developed in fall term. You will be expected to have met 80% of your engineering requirements at this point.

FINAL PEER REVIEW (50 POINTS) - INDIVIDUAL GRADE
Printed copies to Instructor (KEC1148) AND PDF submission to TEACH
All group members will individually prepare a “peer review,” which will be handed in at the end of dead week. In these reviews, students will reflect on their peers’ work and on how well they achieved their goals from the Peer review reflection assignment. Additionally they will reflect on how successful they and their peers were in achieving their goals from the Peer Review reflection assignment. This is due on **5PM on Friday of Dead week (Week 20)**.

**EXTRA CREDIT (?? Points) – INDIVIDUAL GRADING**
Throughout the term, you will be given opportunities to earn extra credit by attending extra lectures and seminars. Based on the content and length of the seminar, a varying amount of extra credit will be given. Watch the Google calendar for these opportunities. Be sure to fill out the sign-up sheet at these events.

**COURSE SCHEDULE**
The course schedule and details of each lecture is available on the ‘Google™ calendar.’ While no changes are expected, please review it periodically to double check.

**IMPORTANT INFORMATION**

**FREE PARTS PROGRAMS**

Analog Devices
- Go to the link below and fill out the form.
- [https://form.analog.com/Form_Pages/corporate/parts.aspx](https://form.analog.com/Form_Pages/corporate/parts.aspx)

National Semiconductor
- Go to the link below.
- Find your part.
- If there is a sample button, send the part number to Donald Heer.
- If there is not a sample button, the part cannot be sampled.

Texas Instruments
- Enter the TI Analog University Design Contest at the link below. Follow the steps to sample parts.

**BEAVERSOURCE**

BeaverSource is a university sponsored tool for project management. At a minimum you will use BeaverSource to organize and display your design specification. You are encouraged however to fully utilize the abilities of the tool since it is likely to make you life easier. Some important things you could look into are the SVN abilities for software, and more advanced use of the ticketing/bug tracking systems.

**DB211 Lab Policies**

Clean-up:
As needed, the graduate TAs will come by the lab at 1pm on Mondays to clean up the lab. Any materials left on a desk not currently occupied will be gently placed into a large box and left near the main door. Exempt items include laptops and appliances. Loose chips and the like will not be spared.

Be Considerate:
We all need to share the room. Please be considerate. Use headphones and shower as to avoid interpersonal conflicts. Do not leave your materials spread all over even if ‘you are only leaving for a few hours’ as the space maybe needed by another group.

Tools and Safety:
A small first aid kit will be attached to the wall near the entry door in the upcoming days. Please only use this kit as needed. Be aware of the tools you are using and turn them off prior to leaving the lab. The tools are a shared resource, if all of the soldering iron tips become damaged due to long term heating, it hurts everyone.