ECE443
SENIOR DESIGN PROJECT

Term: Fall 2012 / Winter 2013 / Spring 2013
Text: Design for Electrical and Computer Engineers
       Ralph M. Ford & Chris S. Coulston

Administrator: Donald Heer
   email: heer@eecs.oregonstate.edu
   phone: x7-2978
   office: KEC1117

COURSE OVERVIEW

ECE441/2/3 is the Electrical Engineering capstone design sequence. The course is intended to follow the engineering design model shown. The cycle is divided out over the various terms with the intention of a finished fully tested project being ready for the engineering expo. Research projects are also possible using the same model.

During ECE441, we will be describing the system level architecture. Once the top-level design is completed, we will continue to design the sub-blocks based on our specifications. While it will not be required, some basic implementation of the individual blocks is suggested as it will help create the design.

In ECE442, We will finish the implementation of the sub-blocks and after each one has be implemented and validated it will be integrated into the system level. Complete validation will not be needed until ECE443, but some of the system requirements will need to be validated during ECE442.

Finally in ECE443, we will finish out the project passing all system validation tests and presenting projects at the Engineering Expo.

It is important to remember that success in this course is your responsibility. Do not depend on the faculty advisor, sponsor, or mentor to keep your project on schedule. Advisors and mentors will support and guide you in completing your project successfully, but you must take the initiative and seek out their help. A successful project is worth your effort and provides a tangible example of your capabilities to potential employers.

COURSE LEARNING OUTCOMES

At the completion of the courses, students will be able to perform the following tasks:
1. Plan, schedule, and carry out an engineering design project.
2. Develop and implement an electrical system using effective design/project techniques.
3. Design and implement test plans and evaluate results.
4. Collaboratively produce written project reports that effectively communicate project information to their target audience(s)—i.e., that are rhetorically appropriate for these audiences and follow disciplinary conventions of usage, vocabulary, format, and citation.
5. Participate effectively in the peer review process.
6. Compose a variety of job-search-related texts, including resumes, cover letters, and professional email communications.
7. Prepare and present formal project-management reviews and other oral presentations.

ABET OUTCOMES
1. Write a concise project description stemming from an identified objective. (ABET outcomes e, f, g)
2. Collect and review technical information on a project from relevant external resources. (ABET outcomes e, j)
3. Project the impact constraints for projects (Resources, Time, Finances) (ABET outcomes d, f)
4. Record technical results and measure progress. (ABET outcomes d, g)
5. Acquire tooling and hardware (components) for a breadboard / prototype. (ABET outcome k)
6. Present project information succinctly to a technically aware audience. (ABET outcomes a, f, g)

WIC Requirements:
7. Develop and articulate content knowledge and critical thinking in the discipline through frequent practice of informal and formal writing.
8. Demonstrate knowledge/understanding of audience expectations, genres, and conventions appropriate to communicating in the discipline.
9. Demonstrate the ability to compose a document of at least 2000 words through multiple aspects of writing, including brainstorming, drafting, using sources appropriately, and revising comprehensively after receiving feedback on a draft.
Academic Dishonesty

At Oregon State University academic dishonesty is defined by the Oregon Administrative Rules 576-015-0020.1.a-c as:

An intentional act of deception in which a student seeks to claim credit for the work or effort of another person or uses unauthorized materials or fabricated information in any academic work.

Academic dishonesty includes:

- **CHEATING** - use or attempted use of unauthorized materials, information or study aids or an act of deceit by which a student attempts to misrepresent mastery of academic effort or information. This includes unauthorized copying or collaboration on a test or assignment or using prohibited materials and texts.

- **FABRICATION** - falsification or invention of any information (including falsifying research, inventing or exaggerating data and listing incorrect or fictitious references.

- **ASSISTING** - helping another commit an act of academic dishonesty. This includes paying or bribing someone to acquire a test or assignment, changing someone's grades or academic records, or taking a test/doing an assignment for someone else (or allowing someone to do these things for you). It is a violation of Oregon state law to create and offer to sell part or all of an education assignment to another person (ORS 165.114).

- **TAMPERING** - altering or interfering with evaluation instruments and documents.

- **PLAGIARISM** - representing the word or ideas of another person as one's own OR presenting someone else's words, ideas, artistry or data as one's own. This includes copying another person's work (including unpublished material) without appropriate referencing, presenting someone else's opinions and theories as one's own, or working jointly on a project, then submitting it as one's own.

IEEE Code of Ethics

As a community of Electrical and Computer Engineers, we have a duty to present ourselves and our profession to each other and the public in the best light possible. The IEEE has a code of Ethics that should always be considered. It reads:

“We, the members of the IEEE, in recognition of the importance of our technologies in affecting the quality of life throughout the world, and in accepting a personal obligation to our profession, its members and the communities we serve, do hereby commit ourselves to the highest ethical and professional conduct and agree:

1. to accept responsibility in making decisions consistent with the safety, health and welfare of the public, and to disclose promptly factors that might endanger the public or the environment;
2. to avoid real or perceived conflicts of interest whenever possible, and to disclose them to affected parties when they do exist;
3. to be honest and realistic in stating claims or estimates based on available data;
4. to reject bribery in all its forms;
5. to improve the understanding of technology, its appropriate application, and potential consequences;
6. to maintain and improve our technical competence and to undertake technological tasks for others only if qualified by training or experience, or after full disclosure of pertinent limitations;
7. to seek, accept, and offer honest criticism of technical work, to acknowledge and correct errors, and to credit properly the contributions of others;
8. to treat fairly all persons regardless of such factors as race, religion, gender, disability, age, or national origin;
9. to avoid injuring others, their property, reputation, or employment by false or malicious action;
10. to assist colleagues and co-workers in their professional development and to support them in following this code of ethics.”
MAJOR ASSIGNMENTS AND PERCENT OF COURSE GRADE

LATE WORK POLICY
All late work will receive no credit. Only pre-discussed exceptions will be accepted.

PEER REVIEW REFLECTION (100 Points) – INDIVIDUAL GRADING
Submitted via TEACH
By the end of week 21, each student will have reviewed and reflected on the peers reviews from the end of the previous term. Based on these reflections, each student will list (BULLETS) a two things they will attempt in order to correct the problems observed (1/2 page). This reflection will be turned into the course instructor via TEACH and a copy given to each group mate. This is due on 5PM on Friday of week 21.

FINAL PROJECT REVIEW (350 POINTS) – GROUP
The final project review is to be held during week 25-26 of the term. Electronic copies of all important datasheets must be on Beaversource before the scheduled review. They should be linked from each block that uses the datasheet. Datasheets for each silicon or electro-mechanical part must be included. Any ‘special’ components not covered by this statement must also have datasheets included. Additionally to get credit for a passed test, there must be proof of that test in the Testing section (section 5) of your Beaversource page.

During a special meeting time in week 25-26, each group will demonstrate their project. Some groups may require more time and will be arranged on an individual basis. During this time, you will show your design, and be asked questions about its operation. You should be prepared to show any of the system tests that you have reported as completed. Your score it based on if your design meets all of the engineering requirements developed in fall term. You will be expected to have met 100% of your engineering requirements at this point.

Additionally, all projects must have at least 50% of components on your own soldered PCB and all parts of all projects must be in an enclosure that satisfies the course instructor that the components are safe and ‘relatively robust.’ Projects presented on breadboards will receive 0 points.

DESIGN EXPOSITION (150 POINTS) – GROUP
Unless prohibited by the project sponsor, all groups are required to participate in the COE Design Exposition held during spring term. Students are to create posters, display their functional prototype, and prepare other supporting material to present and explain their project to fellow students, OSU faculty, industrial representatives, and the general public. The expo is Friday, May 17th from 10am-5pm.

• Contact Card: A business sized card that contains all members names and contact emails. Additionally, the project website, sponsor, and a logo should be included. Your contact card is due via Beaversource and should be linked to Section 9 Expo Materials, on Monday @ 5pm of Week 27. You are responsible for printing your own contact cards for the Expo.
• Poster: Your poster is due via the TEACH interface on Monday @ 5pm of Week 26 and must be posted to Beaversource and should be linked to Section 9 Expo Materials. Posters must be in either MS PowerPoint or Adobe PDF format. The School of EECS will pay for the cost of printing posters that are submitted on time.
• Attendance: Each member of the group should plan to station the booth for at least two hours on the day of the event and the both may not be left unattended. A printed schedule is due to the instructor the day before the Expo @ 5pm.
• Trade Show Goodies: It is not required, but recommended you have some 'Trade Show Goodies' at your booth. This creates a more memorable experience for possible employers. A sample of any ‘candy type’ goodies are due to the instructor the day before the expo 😊.

FINAL PRESENTATION (350 POINTS) - INDIVIDUAL GRADE
Friday @ 5pm of Week 26
The presentations will be a 15 minute recorded presentation with a prototype demonstration. You are responsible for recording your presentation. We are not expecting master video work, but the audio and video should be of a decent quality. This means that voices should be clear compared to other noises and that the video should be of a high enough quality to see all details of the demonstration.

The presentations must be posted to beaver source on your main page and in the presentation section by the deadline. The video must be accessible by clicking on an image from the video.

PEER REVIEW (50 Points) – INDIVIDUAL GRADING
By the end of week 27, each student will have reviewed and reflected on their peer’s Peer Review Reflection from week 21. Based on these reflections, each student will comment on how successful their peer did on each item they were attempting to fix. The format will be a bulleted list addressing each item for each peer. This review will be turned into the course instructor via TEACH and a copy given to each group mate. This is due on **5PM on Friday of week 27.**

**COURSE SCHEDULE**
The course schedule and details of each lecture is available on the ‘Google™ calendar.’ While no changes are expected, please review it periodically to double check.

**IMPORTANT INFORMATION**

**Texas Instruments**
- Enter the TI Analog University Design Contest at the link below. Follow the steps to sample parts.

**BEAVERSOURCE**
Beaversource is a university sponsored tool for project management. At a minimum you will use Beaversource to organize and display your design specification. You are encouraged to fully utilize the abilities of the tool since it is likely to make your life easier. Some important things you could look into are the SVN abilities for software, and more advanced use of the ticketing/bug tracking systems.

**DB211 Lab Policies**

**Clean-up:**
As needed, the graduate TAs will come by the lab at 1pm on Mondays to clean up the lab. Any materials left on a desk not currently occupied will be gently placed into a large box and left near the main door. Exempt items include laptops and appliances. Loose chips and the like will not be spared.

**Be Considerate:**
We all need to share the room. Please be considerate. Use headphones and shower as to avoid interpersonal conflicts. Do not leave your materials spread all over even if ‘you are only leaving for a few hours’ as the space maybe needed by another group.

**Tools and Safety:**
A small first aid kit will be attached to the wall near the entry door in the upcoming days. Please only use this kit as needed. Be aware of the tools you are using and turn them off prior to leaving the lab. The tools are a shared resource. For example, if all of the soldering iron tips become damaged due to long term heating, it hurts everyone.