Lecture 6
Silicon

Announcements

Homework 1/4:
• Due Today.
• Please hand it in at the start of the lecture (10:00am).
• I will return it next Tuesday (October 16th).

Homework 2/4:
• Will be online on Thursday October 11th.
• Due Thursday October 18th at the start of the lecture (10:00am).
• I will return it one week later (October 25th).
• Homework 2 will consist of content covered in Lectures 5, 6 and 7.
Additional Sources

- The course textbook (Brotherton) has a lot of very useful information on this subject (Ch 5-8).
- I also teach a relevant course in Fall odd numbered years (e.g. Fall 2019).
  - Mainly focusing on crystalline silicon for CMOS, but there is a lot of overlap.

Lecture 6

- Amorphous Silicon.
- a-Si:H TFT Fabrication Process.
- a-Si:H TFT Performance.
- Low-Temperature Polycrystalline Silicon.
Mono-Crystalline Silicon

- Single crystal silicon (c-Si) is an established technology.
- It is widely used in microelectronics.
- Why can we not use it for TFT backplanes?
- Traditional manufacturing techniques produce wafers that are 30-45cm diameter. This is not big enough!

https://www.youtube.com/watch?v=aiWywht2HrQ
Mono-Crystalline Silicon

- It would also not cost-effective to make large area (> 2m × 2m) semiconductors.
- Multiple stages involve temperatures > 1000°C.

Amorphous Silicon

- Amorphous silicon (a-Si) is a form of silicon without long-range spatial order.
- It is the dominant incumbent technology for display backplanes.
Amorphous Silicon

- Why is a-Si the incumbent technology?
  - Silicon is well understood (through CMOS technology).
  - Processing facilities exist already for silicon.
  - Cost is relatively low compared to other technologies.
  - a-Si can be deposited over large areas of glass relatively easily.
- However the performance is somewhat low (e.g. mobility \( \sim 1 \text{cm}^2/\text{Vs} \)), and not suited for envisioned next-generation applications (e.g. OLED displays).

Solar Cells

- We will mainly talk about TFTs, but a-Si is also used commercially in solar cells.
Silicon

- Before we talk about disordered silicon, let's first briefly remind ourselves about some details of crystalline silicon.
- Silicon has 14 electrons.
  - 4 in outer shell.

Crystalline Silicon

- Crystalline silicon adopts the diamond structure.
- Each atom has 4 nearest neighbors.
- Tetragonal bonding.
Diamond Cubic

- In its crystalline form, silicon will adopt the diamond cubic structure.
- All atoms are Si (despite colors)!

![](image)

Top-down view

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Number represents height in cell

Bonding in a-Si

- So what happens to bonding when the system is no longer ordered?
- Silicon has 4 outer electrons, so in general wants to bond to 4 other silicon atoms:

![](image)

- The bond distance and tetrahedral angles in c-Si are 2.35 Å and 109.5° respectively.
- In a-Si the RMS deviation from these values are ~2% and ~9-10% respectively.
Bonding in a-Si

- So what happens to bonding when the system is no longer ordered?
- In general there can’t always be 4 bonds per atom:

\[ \text{Si} \leftrightarrow \text{Si} \leftrightarrow \text{Si} \leftrightarrow \text{Si} \]

Dangling bonds

Dangling Bonds

- So how do these dangling bonds effect the electronic properties of silicon?
- It turns out these states are amphoteric.
  - A state capable of trapping electrons or holes.
Dangling Bonds

- This leads to 2 deep states in the band gap.

\[ E_v \]

- These states act as traps to both holes and electrons.
- They significantly hinder the ability of charge carriers to be transported over long distances.

[Diagram showing density of states and energy bands with dangling bonds]

Hydrogenated a-Si

- We can however passivate these states using hydrogen.

- By using ~atomic 10% H, the trap density can be reduced from $10^{20}$ cm$^{-3}$ to $10^{16}$ cm$^{-3}$.
- This has a large influence on transport properties.
- Called hydrogenated amorphous silicon.
- Or a-Si:H.

Hydrogenated Amorphous Silicon TFT Fabrication Process
a-Si:H TFTs

- The most common architecture for an a-Si:H TFT is shown below:

![Diagram showing the architecture of an a-Si:H TFT]

- The reasons this architecture is used are:
  - It operates with acceptable performance for LCD applications.
  - It can be developed at a process temperature of < 350°C.
  - Compatible with large area (>2m \times 2m) deposition.
  - High throughput growth.
  - Requires ≤ 4 masking layers.
  - c.f. > 12 for CMOS.
a-Si:H TFT Fabrication

• The formation of the complete device then proceeds as follows.
• We start with a substrate (conventionally glass).
  • Although we hope to use flexible substrates (e.g. plastic) in the future.
• Normally large areas are used (> 2m × 2m).
• Glass is then cut at some stage in the process.

Backplane Glass

• Glass needs to be high quality (smooth and strong).

https://www.youtube.com/watch?v=q4ZU7zUdM8
**Gate Electrode**

- The gate electrode metal is initially deposited over the entire substrate.
- Normally the metal is **sputtered** onto the glass.
- This allows uniform deposition over large areas.
- Very brief details of sputtering are given here.
- More information can be found in ECE611.

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**Sputtering**

- We need uniform deposition over large areas.

[YouTube Video Link]
Sputtering

- We need uniform deposition over large areas.

The gate electrode then needs to be patterned.
- So that we can apply the gate field to the selected transistor only.
- This is normally carried out via photolithography.
- Again, very brief details of photolithography are given here. More information can be found in ECE611.
The Photolithography Process

- Apply photoresist.
- Expose photoresist through a patterned mask or reticle.
- Develop PR by immersing it in a solvent which preferentially dissolves the PR of higher solubility.
- Process the exposed part of the wafer.
- Strip away the remaining photoresist.
- Inspect pattern.

Silicon Layers

- The next three stages are deposited via chemical vapor deposition (CVD).
- We first deposit amorphous hydrogenated silicon-nitride (a-SiN:H). This is an insulator, and is used as the gate dielectric.
- Next is the undoped a-Si:H. This is our semiconductor.
- Then we deposit n+ doped a-Si:H. This is conducting: acts as our source / drain contacts.
Chemical Vapor Deposition

- Chemical vapor deposition (CVD) is another deposition technique.
- As usual, more details can be found in ECE611.
- In its simplest incarnation, CVD involves flowing a precursor gas or gases into a chamber containing one or more heated objects to be coated.
- Chemical reactions occur on and near the hot surfaces, resulting in the deposition of a thin film on the surface.
- This is accompanied by the production of chemical by-products that are exhausted out of the chamber along with unreacted precursor gases.

Physical Vapor Deposition

- Source material is physically deposited.

Chemical Vapor Deposition

- Involves a chemical reaction.

https://www.youtube.com/watch?v=8mVK5dwycEY
https://www.youtube.com/watch?v=j80jsWFm8Lc
CVD Mechanism

1. Bulk transport
2. Transport across boundary layer
3. Adsorption
4. Surface diffusion
5. Decomposition
6. Reaction with film
7. Diffusion of gaseous by-product
8. Bulk transport of by product

\[ J_1 \propto D_g \Delta C \]

\[ J_2 \propto k_i C_i \]

Silicon Nitride Deposition

Low Pressure CVD (LPCVD at \sim 0.2 to 20 torr)
- Advantages: Excellent uniformity, purity
- Disadvantages: Lower (but reasonable) deposition rates than Atmospheric Pressure CVD (APCVD).
- E.g.:

\[ 3SiCl_2H_2 (G) + 10NH_3 (G) \rightarrow Si_3N_4 (S) + 6NH_4Cl (G) + 6H_2 (G) \]
Etching

• We then have to pattern the individual TFTs to isolate them from each other.
• The photolithography is the same as before.

Metal Deposition

• Next, we need to deposit the metal electrodes.
• These will be patterned during deposition.
• There are many ways to do this.
• Thermal evaporation is one way.
Etching (Again)

- We now need to remove the doped silicon between source and drain electrodes.
- Currently this acts as a shorting pathway between source and drain.
- We can use the source and drain metal contacts as a mask.
- The selectivity between aSi:H and a-Si:H(n+) is very low.
- Etch rate and etch time are very important.

Passivation and Capping

- To complete the device, a final layer of SiN (insulator) is deposited over the entire structure.
- This is to protect the whole structure from exposure to degrading material.
- Contact is made to other parts of the circuit / array via etching or interconnects.
a-Si:H TFT Performance

Crystalline Silicon

- The room-temperature mobility of carriers in monocrystalline silicon is very high.

http://www.ioffe.ru/SVA/NSM/Semicond/Si/electric.html

- This is one reason why it has been so successful for microelectronics.
Amorphous Silicon

- But what happens to carrier mobility when we move to an amorphous system?

- We know electron wavefunctions are no longer coherent.

- What effect does this have on mobility?

Charge Transport in a-Si:H

- Transport in a-Si:H is normally modelled using the Multiple Trapping and Release (MTR) model.
- Recall from last lecture, that MTR describes the system as a mixture of localized and extended states:
MTR

• We saw last time than with the MTR framework the mobility of carriers, $\mu$, can be described by an Arrhenius relationship:

$$\mu = \mu_0 \exp\left(-\frac{E_A}{k_B T}\right)$$

• $\mu$ = mobility of carriers (over long distances).
• $\mu_0$ = mobility prefactor.
• $E_A$ = activation energy.
• $k_B$ = Boltzmann Constant.
• $T$ = Temperature.

Urbach Energy

• When describing the activation energy parameter, it is often easier to evaluate the Urbach Energy, $E_0$.
• This is actually an optical-absorption parameter, and is evaluated from optical data.

• It is essentially a measure of how “broad” the absorption edge is.

\[\text{References:} \quad \text{Tanaka, J. Non-Cryst Sol., 389 (2014) 35.} \]
\[\text{De Wolf, et. al., JPCI, 5 (2014) 1035.} \]
Urbach Energy

- The Urbach energy encapsulates the energetic disorder of both band edges:

\[ E \]

\[ E \]

\[ \text{Density of States} \]

\[ \text{DOS} \]

Activation Energy

- Nonetheless, it is found that Urbach Energy, \( E_0 \), (found by optical spectroscopy) and activation energy, \( E_A \), (found by temperature-dependent TFT measurements) are highly correlated:

\[ E_A \propto E_0 \]

- The mobility is exponentially dependent on activation energy:

\[ \mu = \mu_0 \exp \left( -\frac{E_A}{k_B T} \right) \]

- So the Urbach Energy is often used as a figure of merit for amorphous silicon.
Activation Energy

• The Urbach Energy is found to be strongly dependent on the density of dangling (i.e. unhydrogenated) bonds:

• In the highest quality a-Si:H, the Urbach Energy is $E_0 \approx 50$ meV.

• This corresponds to an activation Energy of $E_A \approx 20$ meV.

Band Mobility

• The other important parameter for MTR is the so-called “band mobility”: $\mu_0$. This is the prefactor in the below equation:

$$\mu = \mu_0 \exp \left( - \frac{E_A}{k_B T} \right)$$

• This the mobility of the extended states in a:Si-H.

• Since the system is amorphous, these are not coherent states.

• The value of $\mu_0$ depends on the scattering length, which is highly dependent on the wavefunction overlap of adjacent transport sites.
Electronic Structure

- To understand the overlap of transport sites in a-Si:H, let us first consider the electronic structure of silicon.
- The ground state electronic structure of silicon is:

\[ Si = 1s^22s^22p^63s^23p^2 \]

- Or:

\[ Si = [Ne]3s^23p^2 \]

- So silicon has 4 valence electrons; 2 in the 3s state, and 2 in the 3p state.

Electron Orbitals

- Within an atom, each electron can be in a finite number of different states, defined by their respective quantum numbers.
- The electron probability distribution can be calculated\(^1\) for each combination of quantum numbers.
- The surface is a position of constant probability density.

\(^1\) A.I.M. Rae., Quantum Mechanics 4\(^{th}\) Edition, IOP Publishing (2002), Chapter 3
Electron Orbitals

- It turns out that the 2s state is spherically symmetric:
- And the 2p state is highly-directional:

[Diagram showing different phases]

- Recall, of the 4 outer electrons in a silicon atom, 2 are in the 2s state, and 2 are in the 2p state.
- In reality these states hybridize.

Electron Orbitals

- The direction of the p-orbitals depends on another quantum number (m), which we will not worry about.
- So really the 2p could look like:

\[ 2p_z \quad 2p_x \quad 2p_y \]
Hybridization

- In an atom, the electrons in an outer shell mix into a **linear combination** of their respective states.
- So instead of 2 electrons in the 2s state and 2 in the 2p state, we have 4 in the sp³ hybridized state.
- In Dirac Notation, we would write wavefunction of an electron as:

\[ |sp^3\rangle = \frac{1}{4}|2s\rangle + \frac{3}{4}|2p\rangle \]

- But the 2p orbital is also separated into 2pₓ, 2pᵧ, and 2pultureInfoz.}

Hybridization

- As with other waves, regions in-phase constructively interfere an out-of phase regions will destructively interfere:

Constructive Interference  Destructive Interference

![Constructive Interference](image1)

![Destructive Interference](image2)
**sp³ Hybridization**

- It turns out that the hybridized \( sp^3 \) orbital will look like the following:

  ![sp³ Hybridization Diagram](image)

- And it turns out 4 \( sp^3 \) orbitals combined will have **tetrahedral angles of 109.5°**.

- This is energetically the most favorable state.

**Crystalline Silicon**

- The p-type component of the orbitals are in-phase and contribute to bonding.
- This leads to the observed silicon crystal structure.

https://youtu.be/ApqFLVd0XaI?t=9m10s
Electronic Structure

• Recall, the RMS deviations in bond length and bond angle are only ~2% and 10% respectively:

![Graph 1](image1.png)

![Graph 2](image2.png)

• What does this mean for electronic structure?

Electronic Structure

• It turns out these deviations correspond to only a 0.1eV deviation from the 2.5eV bond strength found in c-Si.

• The density of states can therefore be calculated in a similar way as for c-Si.
Electronic Structure

- Electron transport is associated with s-type orbitals (spherical).
- Hole transport is associated with p-type orbitals (directional).

- The directional p-type states are more effected by bond disorder.
  - This leads to a greater energetic disorder.
  - This in turn leads to a higher $E_A$ and lower $\mu_0$.
- In a-Si:H TFT the electron mobility is found to be higher than the hole mobility.
Typical Mobilities

• General ranges of MTR parameters for low-dangling-bond-density a-Si:H are:
  • $E_A \sim 20 – 35$ meV.
  • $\mu_0^e \sim 10 – 20$ cm$^2$/Vs.   • $\mu_0^{h^+} \sim 1 – 10$ cm$^2$/Vs.
  • So normally, field-effect mobilities in a-Si:H are typically around:
    • $\mu \sim 0.5 – 1$ cm$^2$/Vs for electrons.
    • $\mu \sim 0.005 – 0.01$ cm$^2$/Vs for holes.
  • So a-Si:H TFTs are almost exclusively n-type only.

Low-Temperature Polycrystalline Silicon (LTPS)
Polycrystalline Silicon

- We know we cannot use c-Si because: wafers are too small and thermal budget is too high.
- While a-Si:H TFTs are routinely used, we also know the mobility is not high-enough for next generation products (e.g. OLED displays).
- So what then about meeting in the middle, and using polycrystalline silicon (poly-Si)?

Polycrystalline Films

- What do we mean by polycrystalline silicon?
- Basically we have many regions of fully ordered crystalline silicon.
- However these regions all have different crystallographic orientations separated by grain boundaries.
- Grain boundaries limit performance.
Polycrystalline Films

- How do we make poly-Si thin films?
- Electronic Grade Polysilicon (EGS) is actually used as a precursor for single-crystal silicon.

- Very large thermal budget!
- We seek low-temperature poly-Si (LTPS); ≤ 650°C.

Direct Deposition via LPCVD

- Originally poly-Si was grown using a similar approach to a-Si:H; low-pressure chemical vapor deposition (LPCVD).
- However, to get polycrystalline silicon, rather than amorphous, we use temperatures above >600°C.
  - Even for glass this can lead to warping. No chance with plastic!
  - Grain size ~100nm.
  - Leading to mobilities ~5-7 cm²/Vs.
Solid-Phase Crystallization

- For these reasons, direct deposition of poly-Si was quickly abandoned as a strategy.
- Instead a-Si was deposited at lower temperatures (~350°C), as described earlier.
- The films were then thermally annealed to induce solid-phase crystallization (SPC).
  - Temperatures: 580 – 630°C.
  - Annealing times of up to 10 hours.
  - Large dendritic grains are formed.
  - Electron mobilities up to 40 cm²/Vs.

Solid-Phase Crystallization

- The long exposure time is even worse for glass substrates than direct deposition.
- Even though the glass does not melt, its structure is significantly affected.
- This leads to issues with mask-alignment.
- E.g. for a 30cm substrate, with 3 μm alignment tolerance, we need to maintain a stability of 10ppm from first to last alignment stage.
- Glass needs to be pre-shrunk before first alignment.
Excimer Laser Annealing

- Although mobilities were good with SPC, the high thermal budget, and issues with glass deformation meant SPC was not attractive for industrialization.
- The third generation process is the industrial standard: **excimer laser annealing (ELA)**
- Here we use a laser to melt the a-Si.
- Under the correct conditions it will re-solidify in a polycrystalline form.

Excimer Lasers

- Ultraviolet lasers are used:
  - XeCl: 308nm, (4.03 eV).
  - KrF: 248nm, (5.00 eV).
- The XeCl laser is normally used in industry as it is less damaging to optical components in the beam path.
- The pulse duration is ~30ns, and the repetition rate can be up to 600 Hz.
- The energy density is pretty high; up to ~1 J/pulse.
  - ~$10^{18}$ photons per pulse.
Excimer Lasers

- The raw laser shape is Gaussian, but the ideal shape is pencil-shaped.
- This is achieved with optics:

![Diagram of excimer laser setup](image)

- The laser is pulled across the sample surface.

Heating Silicon

- At 308nm the absorption depth of a-Si is only 7.6nm.
- So a large percentage of photons are absorbed.
- At high fluence (photon density) the silicon will be intensely heated.
- Above $T_m = 1420K$ the silicon will begin to melt.
- If done quickly and controllably, the silicon should re-crystallize into LTPS without damaging the underlying substrate.
- Unsurprisingly, the pulse energy has a huge impact on microstructure.
Molten Silicon

• It turns out there is a sweet point when melting silicon to get maximum grain size.

During irradiation

(i) $E < E_{\text{melt}}$ – partial melting

(ii) $E = E_{\text{melt}}$ – near melt-through

(iii) $E > E_{\text{melt}}$ – full melt-through

Crystallised film

- Medium grain

- Fine grain/ amorphous

Nucleation on solid regions

Super lateral growth (SLG) (I'm et al.)

Random nucleation in super cooled melt.

Fine grain

This is evidenced by the average grain radius:
**Molten Silicon**

- And by TFT mobility:
  
  ![Mobility vs Energy Density Graph](image)

  Fig 7.6. Brotherton

**Performance**

- Let’s look at some transfer curves:

- The mobility in LTPS is **very high** for a thin-film material: > 100 cm²/Vs.

- We also can dope the material to be p-type or n-type.
- A requirement for complementary logic.
- The on/off ratio is not bad.
The Big Problem with LTPS

- So why is LTPS not widespread?

Non-Uniformity

- By its nature, polycrystalline silicon is very inhomogeneous.
- Device-to-device variation is very large indeed.
- In particular channel length-dependence.
Non-Uniformity

- Device-to-device variation is a really big problem.
- It requires more complex pixel-driver circuits.
- And results in lower yield.

a-Si:H vs LTPS

- So how do the two silicon-based technologies compare?

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<th>a-Si:H</th>
<th>LTPS</th>
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Next Time...

- Metal Oxide Semiconductors/