Useful Constants:

<table>
<thead>
<tr>
<th>Name</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vacuum Permittivity</td>
<td>$\varepsilon_0$</td>
<td>$8.85 \times 10^{-12}$ F/m</td>
</tr>
<tr>
<td>Fundamental Unit of Charge</td>
<td>$e$</td>
<td>$1.60 \times 10^{-19}$ C</td>
</tr>
<tr>
<td>Boltzmann Constant</td>
<td>$k_B$</td>
<td>$1.38 \times 10^{-23}$ J/K</td>
</tr>
<tr>
<td>Planck Constant</td>
<td>$h$</td>
<td>$6.63 \times 10^{-34}$ Js</td>
</tr>
<tr>
<td>Pi</td>
<td>$\pi$</td>
<td>3.14</td>
</tr>
<tr>
<td>Rest Mass of Electron in Vacuum</td>
<td>$m_e$</td>
<td>$9.11 \times 10^{-31}$ kg</td>
</tr>
<tr>
<td>Speed of light in vacuum</td>
<td>$c$</td>
<td>$3.00 \times 10^8$ m/s</td>
</tr>
</tbody>
</table>

Useful Equations:

Capacitance per Unit Area of Parallel Plate Capacitor:

$$ C = \frac{\varepsilon_0 \kappa}{d} $$

- $C$ is the capacitance per unit area.
- $\varepsilon_0$ is the vacuum permittivity.
- $\kappa$ is the relative permittivity.
- $d$ is the separation distance of the plates.

Gate-Induced Mobile Charge Density in TFT:

$$ Q_{mob} = C(V_G - V_T) $$

- $Q_{mob}$ is the areal charge density of induced carriers.
- $C$ is the capacitance per unit area.
- $V_G$ is the applied gate voltage.
- $V_T$ is the TFT threshold voltage.

Characteristic Energy of Metal Semiconductor Interface:

$$ E_{00} = \frac{e h}{4 \pi} \sqrt{\frac{n}{\varepsilon_0 \varepsilon_r m_{tun}^*}} $$

- $E_{00}$ is the characteristic energy of the interface.
- $e$ is the fundamental unit of charge.
- $h$ is the Planck Constant.
- $n$ is the free carrier density in the semiconductor.
- $\varepsilon_0$ is the vacuum permittivity.
- $\varepsilon_r$ is the relative permittivity of the semiconductor.
- $m_{tun}^*$ is the effective mass of tunneling.
Energy of Photon:

\[ E = \frac{hc}{\lambda} \]

- \( E \) is the photon energy.
- \( h \) is the Planck Constant.
- \( c \) is the speed of light in a vacuum.
- \( \lambda \) is the wavelength of the light.

Relationship between Frequency and Wavelength of Light:

\[ v = \frac{c}{\lambda} \]

- \( v \) is the photon frequency.
- \( c \) is the speed of light in a vacuum.
- \( \lambda \) is the wavelength of the light.

Binding Energy of Electrons as Determined by Ultraviolet Photoemission Spectroscopy:

\[ E_B = hv - KE - e\phi_{sp} \]

- \( E_B \) is the binding energy of photo-emitted electrons.
- \( h \) is the Planck Constant.
- \( v \) is the photon frequency of incident UV photons.
- \( KE \) is the kinetic energy of detected electrons.
- \( e \) is the magnitude of the fundamental unit of charge.
- \( \phi_{sp} \) is the workfunction of the detector in Volts.

Smits Model for n-type Unipolar TFT:

\[ I_D = \gamma \frac{W}{L} \frac{T}{2T_0} \frac{T}{2T_0 - T} \left[ (V_G - V_T)^{2T_0/T} - (V_G - V_T - V_D)^{2T_0/T} \right] \]

- \( I_D \) is the source-drain current.
- \( \gamma \) is the gamma parameter for electrons in this semiconductor.
- \( W \) is the transistor channel width.
- \( L \) is the transistor channel length.
- \( T \) is the temperature.
- \( T_0 \) is the characteristic temperature describing the width of electron states of this semiconductor.
- \( V_G \) is the applied gate voltage.
- \( V_T \) is the threshold voltage.
- \( V_D \) is the applied drain voltage.

Smits Model for p-type Unipolar TFT:

\[ I_D = \gamma \frac{W}{L} \frac{T}{2T_0} \frac{T}{2T_0 - T} \left[ (V_T - V_G)^{2T_0/T} - (V_T - V_G + V_D)^{2T_0/T} \right] \]

- \( I_D \) is the source-drain current.
- \( \gamma \) is the gamma parameter for holes in this semiconductor.
- \( W \) is the transistor channel width.
- \( L \) is the transistor channel length.
• $T$ is the temperature.
• $T_{0e}$ is the characteristic temperature describing the width of hole states of this semiconductor.
• $V_G$ is the applied gate voltage.
• $V_T$ is the threshold voltage.
• $V_D$ is the applied drain voltage.

Smits Model for Ambipolar TFT with Electron Majority Carriers:

$$I_D = \frac{W}{L} \left[ \gamma_e \frac{T}{2T_{0e}} - \frac{T}{T - T_{0e}} (V_G - V_T)^{2T_{0e}/T} + \gamma_h \frac{T}{2T_{0h}} - \frac{T}{T - T_{0h}} (V_D - V_G + V_T)^{2T_{0h}/T} \right]$$

• $I_D$ is the source-drain current.
• $W$ is the transistor channel width.
• $L$ is the transistor channel length.
• $T$ is the temperature.
• $\gamma_e$ is the gamma parameter for electrons in this semiconductor.
• $\gamma_h$ is the gamma parameter for holes in this semiconductor.
• $T_{0e}$ is the characteristic temperature describing the width of electron states of this semiconductor.
• $T_{0h}$ is the characteristic temperature describing the width of hole states of this semiconductor.
• $V_G$ is the applied gate voltage.
• $V_T$ is the threshold voltage.
• $V_D$ is the applied drain voltage.

Smits Model for Ambipolar TFT with Hole Majority Carriers:

$$I_D = \frac{W}{L} \left[ \gamma_h \frac{T}{2T_{0h}} - \frac{T}{T - T_{0h}} (V_T - V_G)^{2T_{0h}/T} + \gamma_e \frac{T}{2T_{0e}} - \frac{T}{T - T_{0e}} (V_T - V_G + V_D)^{2T_{0e}/T} \right]$$

• $I_D$ is the source-drain current.
• $W$ is the transistor channel width.
• $L$ is the transistor channel length.
• $T$ is the temperature.
• $\gamma_e$ is the gamma parameter for electrons in this semiconductor.
• $\gamma_h$ is the gamma parameter for holes in this semiconductor.
• $T_{0e}$ is the characteristic temperature describing the width of electron states of this semiconductor.
• $T_{0h}$ is the characteristic temperature describing the width of hole states of this semiconductor.
• $V_G$ is the applied gate voltage.
• $V_T$ is the threshold voltage.
• $V_D$ is the applied drain voltage.

External Quantum Efficiency of Phototransistor:

$$\eta = \frac{(I_{D,ill} - I_{D,dark})hc}{eP_LW}$$

• $\eta$ is the external quantum efficiency (EQE) of the phototransistor. EQE is between 0 and 1.
• $I_{D,ill}$ is the source-drain current under illumination.
• $I_{D,dark}$ is the source-drain current in the dark.
• \( h \) is the Planck Constant.
• \( c \) is the speed of light in a vacuum.
• \( e \) is the fundamental unit of charge.
• \( P_I \) is the optical power density incident on the transistor channel.
• \( W \) is the transistor channel width.
• \( L \) is the transistor channel length.

**Strain:**

\[
\varepsilon = \frac{L_n - L_0}{L_0}
\]

• \( \varepsilon \) is the strain in the deformation direction.
• \( L_0 \) is the original object length.
• \( L_n \) is the object length after deformation.

**Stress:**

\[
\sigma = \frac{F}{A}
\]

• \( \sigma \) is the stress in the direction of applied force
• \( F \) is the force applied to the object.
• \( A \) is the cross-sectional area of the object.

**Young’s Modulus:**

\[
Y = \frac{\sigma}{\varepsilon}
\]

• \( Y \) is the Young’s modulus of the material.
• \( \sigma \) is the stress in the direction of applied force
• \( \varepsilon \) is the strain in the deformation direction.
**Question 1 [10 marks]:**

a) The Figure below shows some example TFT transfer data. Assume that $I_D$ is the source-drain current, and $I_G$ is the source-gate leakage current. If the transistor source electrode has an area of 0.005 cm$^2$, what is the maximum leakage current density measured? Give your answer in A/cm$^2$. [2 mark]

Here we basically just need to convert current to current density. We are told we can approximate $I_G$ as the source-gate current, and hence do not need to consider current flowing between the drain and the gate. This is also implicit, since at $V_G = 120V$, the difference between drain and gate potentials is close to zero and hence very little current should flow between them.

From the figure we can read-off the maximum gate leakage current as $2 \times 10^{-5}$ A. We are told in the question that the source electrode is 0.005 cm$^2$. So the leakage current density is simply:

$$J = \frac{I}{A} = \frac{2 \times 10^{-5}}{0.005} = 4 \text{ mA/cm}^2$$

b) The figure below shows the current measured as a function of applied voltage for a metal-insulator-metal capacitor with an 80nm thick insulator layer. The red arrows indicate the measurement direction. From this data, approximate the breakdown field strength. Give your answer in MV/cm. If this breakdown process was reversible, state what differences you would expect to see in this figure.[3 marks]
This is another very simple problem that you have seen before. We just need to identify the voltage at which breakdown occurs, and calculate the corresponding electric field strength. We are told the dielectric is 80nm thick and we can see from the figure that the dielectric breaks down at 4V. The breakdown field strength is therefore:

\[ E_b = \frac{V}{d} = \frac{4}{8 \times 10^{-6}} = 0.5 \text{ MV/cm} \]

If the breakdown was reversible we would expect the forward and reverse sweeps (as defined by the arrows) to overlap.

c) Consider the self-assembled monolayer: octadecyl-acrylamide (ODA), whose molecular structure is shown in the figure below. If ODA was used as a gate dielectric on its own (i.e. not on top of Al\textsubscript{2}O for example), calculate the voltage required to induce a mobile carrier number density of \(1.1 \times 10^{13}\) cm\(^{-2}\). Assume the threshold voltage for this TFT is zero and the relative permittivity of this molecule is \(\kappa = 3\). For this calculation you can approximate all carbon atoms as being in a straight line with a carbon-carbon and carbon-nitrogen bond length of 150 pm, and you can neglect hydrogen atoms. Explain why this is likely to be an over-estimate of the operation voltage.\[4\text{ marks}\]

This is a question about calculating capacitance, and from that calculating charge density. So we first need to count the number of atoms in the line. Looking at the molecule above, we see there are 21 atoms (20 carbon, 1 nitrogen). This means there are 20 atomic bonds in a row. We are told we can approximate the atoms to a straight line. So we can approximate the molecule as having the following length:

\[ d = 150 \times 10^{-12} \times 20 = 3 \text{ nm} \]
We can now evaluate the capacitance per unit area:
\[
C = \frac{\varepsilon_0 \kappa}{d}
\]

We are given the vacuum permittivity in the useful constants and told the relative permittivity of the molecule is: \( \kappa = 3 \). Work in SI units because we have a fundamental constant with SI units:
\[
C = \frac{8.85 \times 10^{-12} \times 3}{3 \times 10^{-9}}
\]
\[
C = 8.85 \times 10^{-3} \text{ F/m}^2
\]

We can convert to F/cm here:
\[
C = 8.85 \times 10^{-7} \text{ F/cm}^2
\]

Now we just need to now evaluate the carrier density. We are also given the equation for induced mobile charge carrier density:
\[
Q_{mob} = C(V_G - V_T)
\]

We are told the threshold voltage in our TFT is \( V_T = 0 \) V, so we can immediately simplify this to:
\[
Q_{mob} = CV_G
\]

This is the charge density, however we are interested in an areal number density (\( n_{mob} \)). Each charge carrier carries a charge of \( e \), so we can say:
\[
n_{mob} = \frac{Q_{mob}}{e}
\]

I.e.:
\[
n_{mob} = \frac{CV_G}{e}
\]

We seek applied gate voltage:
\[
V_G = \frac{en_{mob}}{C}
\]

We are told the target carrier density is \( 1.1 \times 10^{13} \text{ cm}^{-2} \). Hence we can now just enter numbers:
\[
V_G = \frac{1.6 \times 10^{-19} \times 1.1 \times 10^{13}}{8.85 \times 10^{-7}}
\]
\[
V_G = 199 \text{ V}
\]
In reality we can see from the figure shown that the bond angles are not 180 between atoms. For this reason 3nm is probably an over-estimate of the length. If we are overestimating the dielectric thickness (molecule length) then we are under-estimating capacitance. If we are under-estimating capacitance, then we are over-estimating operation voltage.

d) Provide a possible explanation for the observation that metal-oxide TFTs employing high-κ dielectrics such as HfO$_2$ or ZrO$_2$ exhibit higher charge-carrier mobilities than those employing conventional dielectrics such as SiO$_2$ for example.

This is currently a matter of debate in the community, however there is some evidence that charges transferred from the high-κ dielectric material can pre-fill traps in the some metal oxide thin film semiconductors.

**Question 2 [9 marks]:**

a) In the context of semiconductor-metal interfaces, we consider field emission dominant if the characteristic energy of the semiconductor is over 5× the thermal energy. For an interface with an effective mass of tunneling of 0.3$m_e$, a semiconductor carrier density of $n = 4.47 \times 10^{17}$, and a semiconductor relative permittivity of 11.7, determine the temperature below which field emission dominates. $m_e$ is the rest mass of an electron. Give you answer in Kelvin.

From the question we understand that the onset of field emission occurs when $E_{00} = k_BT$. we just need to evaluate the temperature at which this condition is met:

$$E_{00} = \frac{eh}{4\pi} \sqrt{\frac{n}{\varepsilon_0 \varepsilon_r m_t^*}} = k_BT$$

$$T = \frac{eh}{4\pi k_B} \sqrt{\frac{n}{\varepsilon_0 \varepsilon_r m_t^*}}$$

This is just an exercise in entering numbers. Since there are so many fundamental constants we will just work in SI. Hence we need to convert $n$ from cm$^{-3}$ to m$^{-3}$:

$$n = 4.47 \times 10^{17} \text{ cm}^{-3}$$

$$n = 4.47 \times 10^{23} \text{ cm}^{-3}$$

Evaluate the fraction out the front first:

$$\frac{eh}{4\pi k_B} = \frac{1.6 \times 10^{-19} \times 6.63 \times 10^{-34}}{4 \times 3.14 \times 1.38 \times 10^{-23}} = 6.13 \times 10^{-31}$$

Now evaluate the fraction in the root:

$$\frac{n}{\varepsilon_0 \varepsilon_r m_t^*} = \frac{4.47 \times 10^{23}}{8.85 \times 10^{-12} \times 11.7 \times 0.3 \times 9.11 \times 10^{-31}} = 1.58 \times 10^{64}$$

We can then evaluate the temperature:
\[ T = 6.13 \times 10^{-31} \times \sqrt{1.58 \times 10^{64}} \]

\[ T = 77K \]

b) Describe briefly the difference between conventional resistivity and specific interfacial resistivity. [2 marks]

Conventional resistivity is a bulk property that encapsulates the ability of current to flow through a 3-dimensional material for a particular applied voltage across it. Specific interfacial resistivity is an analogous property, that encapsulates the resistance / conductance properties of a 2-dimensional interface, rather than a 3-dimensional volume. The former is conventionally quoted in units of \( \Omega \text{cm}^{-1} \), while the later is conventionally quoted with units of \( \Omega \text{cm}^{-2} \).

c) An ultraviolet-visible (UVVis) spectroscopic absorption measurement is carried out on a semiconductor, and the material is observed to have an onset of absorption of 776 nm. An ultraviolet photoelectron spectroscopy (UPS) measurement is carried out on the same sample. During this UPS experiment, the longest-wavelength incident photons which result in photoelectron emission are 116 nm. At this wavelength of incident photons, electrons are emitted with a kinetic energy of 100 meV. The workfunction of the detector is 5.1V. Using this information, draw the band diagram of this semiconductor, labeling the conduction band minimum, the valence band maximum, and the band gap. Quote these energies in electron volts. [4 marks]

There are two parts to this question. The first is to determine the band gap of the semiconductor. Normally UVVis spectroscopy will be carried out, then Tauc analysis would be used to determine approximately the onset of absorption, which can in turn be used to determine the band gap of the semiconductor. Instead here we are told the absorption onset is 776 nm. To determine the band gap we hence just need to convert photon wavelength into energy:

\[ E = \frac{hc}{\lambda} = \frac{6.63 \times 10^{-34} \times 3 \times 10^8}{776 \times 10^{-9}} = 2.56 \times 10^{-19}J = 1.6 \text{ eV} \]

The valence band maximum can be evaluated from the UPS experiment. When carrying out a UPS experiment, the binding energy of detected electrons is expressed using the following equation:

\[ E_B = h\nu - KE - e\phi_{sp} \]

This tells us the binding energy of a particular electron. We can assume that the energy of the top of the valence band is equal to the binding energy of the most weakly-bound electrons (by definition). We are told that the lowest energy photons that result in photo-emission have a wavelength of 116nm. Since the equation for binding energy requires a photon frequency (\( \nu \)) rather than a wavelength (\( \lambda \)), we use the relationship between photon frequency and photon wavelength:

\[ \nu = \frac{c}{\lambda} \]
\[ E_B = \frac{hc}{\lambda} - KE - e\phi_{sp} \]

We now just need to enter the relevant numbers. As usual, we will stick to SI while using fundamental constants:

\[ E_B = \frac{6.63 \times 10^{-34} \times 3 \times 10^8}{116 \times 10^{-9}} - 0.1 \times 1.60 \times 10^{-19} - 1.60 \times 10^{-19} \times 5.1 \]

\[ E_B = 1.71 \times 10^{-18} - 1.60 \times 10^{-20} - 8.17 \times 10^{-19} \]

\[ E_B = 8.81 \times 10^{-18} \]

\[ E_B = 5.50 \text{ eV} \]

So we now know the band gap is 1.5 eV and the valence band maximum is 5.5 eV. We can hence infer that the conduction minimum is 4.0 eV. This allows us to construct the following band diagram:

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**Question 3 [8 marks]:**

a) We are designing a light-emitting transistor based on an ambipolar semiconductor. The TFT has a threshold voltage for electrons of \( V_{Te} = +5 \text{ V} \) and a threshold voltage for holes of \( V_{Th} = -7 \text{ V} \). If you choose to apply a gate voltage of \( V_G = -40 \text{ V} \), state what range of drain voltages would result in light emission.[3 marks]

So the first thing to identify about this question is that for light emission to take place we require that both carriers are present in the channel at the same time. We will assume that the voltage conditions for both carriers to be present are the same as those for light emission. I.e. the question is asking what voltages are required for both carriers to be present in the channel at the same time.

We are applying a negative gate bias, and therefore we know holes are the majority carrier. This is because the gate bias is more negative than the threshold voltage for holes:

\[ |V_G| > |V_{Th}| \]
The first criterion for both carrier types to be present in the channel is that the channel is saturated to the majority carrier (holes in our case). We know from descriptions of unipolar TFTs that for this to be the case for holes, we require:

\[ V_D < V_G - V_{Th} \]

We are told the threshold voltage for holes is \( V_{Th} = -7 \text{V} \) and the applied gate bias is \( V_G = -40 \text{V} \). I.e. for the channel to be saturated we require:

\[ V_D < -40 - 7 \]

I.e.:

\[ V_D < -33 \text{ V} \]

To know whether or not we have electron injection from the drain terminal, we have to reconsider the biases relative to this terminal. I.e. we need to carry out a voltage transformation. Sometimes it is easier to draw a picture to visualize the transformation:

So looking from the prospective of the drain (D) electrode, we need the relative voltage at the gate to be higher than the threshold voltage for injection for electrons. I.e. we need:

\[ V_G - V_D > V_{Te} \]

Always be careful when changing variable sign in inequalities:

\[ V_G - V_D > V_{Te} \]

\[ -V_D > V_{Te} - V_G \]

\[ V_D < V_G - V_{Te} \]

We are told both the applied gate voltage and the threshold voltage for electrons:

\[ V_D < -40 - 5 \]

\[ V_D < -45 \text{ V} \]

So to see both holes and electrons in the channel we require that both the following inequalities are obeyed:
\[ V_D < -33 \text{ V} \]
\[ V_D < -45 \text{ V} \]

The second inequality makes the first redundant, so we can hence say for light emission in this TFT we require:

\[ V_D < -45 \text{ V} \]

b) A narrow-band-gap semiconductor is employed in two TFTs. In the first TFT, the electrodes only allow the injection and transport of holes. In the second TFT, both holes and electrons can be injected and transported. Use the parameters in the table below to determine the difference in measured source-drain current between the two TFTs, if one were to apply a gate and drain voltage of \( V_G = -20 \text{ V} \) and \( V_D = -10 \text{ V} \), respectively. The temperature is 300K, and the channel length and width are \( L = 10 \mu \text{m} \), and \( W = 10 \text{ mm} \) respectively. You can assume the threshold voltage for holes and electrons are both zero, for both TFTs.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Electrons</th>
<th>Holes</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \gamma ) (A)</td>
<td>( 3.45 \times 10^{-15} )</td>
<td>( 1.57 \times 10^{-15} )</td>
</tr>
<tr>
<td>( T_0 ) (K)</td>
<td>460</td>
<td>600</td>
</tr>
</tbody>
</table>

As long as you identify correctly what the question is asking, this is just an exercise in entering numbers. Since we are talking about ambipolar TFTs we need to use the Smits model to accurately describe the devices.

Start by evaluating the current for a device in-which we know only holes can flow. In this case, we use the equation for a unipolar hole-transporting TFT:

\[
I_D = \gamma \frac{W}{L} \frac{T}{2T_0} \frac{T}{T_0 - T} \left( (V_T - V_G)^{2T_0/T} - (V_T - V_G + V_D)^{2T_0/T} \right)
\]

We are told the threshold voltage is zero in all cases, so we can simply this slightly:

\[
I_D = \gamma \frac{W}{L} \frac{T}{2T_0} \frac{T}{T_0 - T} \left( (-V_G)^{2T_0/T} - (-V_G + V_D)^{2T_0/T} \right)
\]

We are given the parameters in the question and table:

\[
I_D = 1.57 \times 10^{-15} \times \frac{10000}{10} \times \frac{300}{2 \times 600} \times \frac{300}{2 \times 600 - 300} \left[ (20)^{2 \times 600/300} - (20 - 10)^{2 \times 600/300} \right]
\]

\[
I_D = 1.57 \times 10^{-15} \times 1000 \times \frac{300}{1200} \times \frac{300}{1200 - 300} \left[ (20)^{1200/300} - (20 - 10)^{1200/300} \right]
\]

\[
I_D = 1.57 \times 10^{-12} \times \frac{11}{43} \left[ (20)^4 - (10)^4 \right]
\]

\[
I_D = 1.97 \times 10^{-8} \text{ A}
\]

\[
I_D = 19.7 \text{ nA}
\]
A similar approach can be taken for the ambipolar TFT, but in this case the following equation should be used:

\[
I_D = \frac{W}{L} \left[ y_h \frac{T}{2T_{oh}} \frac{T}{2T_{oh}} (V_T - V_G) 2^{T_{oh}/T} + y_e \frac{T}{2T_{oe}} \frac{T}{2T_{oe}} (V_T - V_G + V_D) 2^{T_{oe}/T} \right]
\]

Recall we have zero threshold voltage:

\[
I_D = \frac{W}{L} \left[ y_h \frac{T}{2T_{oh}} \frac{T}{2T_{oh}} (-V_G) 2^{T_{oh}/T} + y_e \frac{T}{2T_{oe}} \frac{T}{2T_{oe}} (-V_G + V_D) 2^{T_{oe}/T} \right]
\]

Here we again, just enter the numbers:

\[
I_D = \frac{10000}{10} \left[ 3.45 \times 10^{-15} \times \frac{300}{2 \times 460} \frac{300}{2 \times 460} \frac{300}{300} (20)^{2 \times 460/300} \\
+ 1.57 \times 10^{-15} \times \frac{300}{2 \times 600} \frac{300}{2 \times 600} \frac{300}{300} (20 - 10)^{2 \times 600/300} \right]
\]

It turns out that in this case:

\[
I_D = 20.3 \text{nA}
\]

So the difference in source drain current is:

\[
\Delta I_D = 2.03 \times 10^{-8} - 1.97 \times 10^{-8} = 6 \times 10^{-10} = 600 \text{ pA}
\]

c) When designing a light-emitting transistor, which architecture would be logical to choose? A bilayer TFT or a blend TFT? Explain why.[2 marks]

The critical thing here to remember is that for light to be emitted we need holes and electrons to come into contact with each other. I.e. they need to be present in the same semiconductor at the same time. Bilayer ambipolar TFTs are designed to have electrons in one channel and holes in the other. While it is possible for carriers to cross the interface between the two semiconductors, it is not the optimized structure for recombination. A blend TFT on the other-hand, where two semiconductors inter-penetrete on very small length scales (often ~1nm) is a structure where both electrons and holes share the same channel. This could be described as a conventional ambipolar TFT, with a single position in-which carriers recombine. For this reason a **blend TFT is the more logical choice** for light-emission.

**Question 4 [7 marks]:**

a) The figure below shows the characteristics of two phototransistors: Phototransistor A and phototransistor B. Using these characteristics, decide which phototransistor is more likely to have its photocurrent enhancement due to the photoconductive effect and which is more likely to be due to the photovoltaic effect. Explain your answer.[2 marks]
We notice that upon illumination, TFT A undergoes a shift in threshold voltage. This is characteristic of a change in trapped charge density at the semiconductor-dielectric interface and termed the photovoltaic effect.

Upon illumination, the off-current of TFT B increases significantly but the on current does not really change as much. This is a behavior associated with direct charge generation and extraction, and is called the photoconductive effect.

b) A phototransistor, with a length of $L = 10 \mu$m, and width of $W = 1000 \mu$m is held at constant gate and drain voltages and illuminated with pulsed green light. The figure below shows the optical power density applied to the phototransistor as a function of time (top), and the measured source-drain current of the phototransistor. From this data determine the external quantum efficiency of this device at these applied biases and illumination intensity. Give your answer in %. [3 marks]
Here we just need to evaluate the EQE by entering numbers into the equation. The only difficulty is correctly identifying parameters from the above graph. The equation for EQE is given at the start of the document:

\[ \eta = \frac{(I_{D,ill} - I_{D,dark})hc}{eP_iLW} \]

At lot of these parameters are constants: \( h, c, \) and \( e, L \) and \( W \) are given. We just need to determine \( I_{D,ill} \) \( I_{D,dark} \) and \( P_i \). The scale of the \( x \) axis is irrelevant; it just tells when the light is on or off. We see the low of the top square wave is 0 mW/cm\(^2\); hence this is when the device is in the dark. Looking at the corresponding current below we can identify that when the device is off the source-drain current is: 0.2 mA. i.e. we can say: \( I_{D,dark} = 2 \times 10^{-4} \) A.

At the top of the square wave the optical power density is \( P_i = 2 \) mW/cm\(^2\). Under this illumination we see that the source-drain current that flows is: \( I_{D,ill} = 1.8 \times 10^{-3} \) A.

Now we just have to enter values. Since there are a few fundamental constants it is probably easier to just convert everything to SI:

\[ L = 10 \ \mu m = 10 \times 10^{-6} \ m = 10^{-5} \ m \]
\[ W = 1000 \ \mu m = 1000 \times 10^{-6} \ m = 10^{-5} \ m \]
\[ P_i = 2 \ mW/cm^2 = 0.002 \ W/cm^2 = 200 \ W/m^2 \]

Now we can enter numbers:

\[ \eta = \frac{(1.8 \times 10^{-3} - 2 \times 10^{-4}) \times 6.63 \times 10^{-34} \times 3.00 \times 10^8}{1.60 \times 10^{-19} \times 20 \times 10^{-5} \times 10^{-5}} \]
\[ \eta = \frac{3.18 \times 10^{-28}}{3.20 \times 10^{-26}} = 9.95 \times 10^{-3} \]

This is just a number between 0 and 1. We are asked for the EQE as a percentage, i.e.:

\[ \eta = 0.995\% \approx 1\% \]

c) Explain why it is possible to have a phototransistor with an external quantum efficiency above 100\%.[2 marks]

For a device that relies upon direct charge generation (e.g. a photodiode or a phototransistor that relies entirely upon the photoconductive effect), it is impossible to generate more energy in charge than provided by energy that enters as photons. This would violate the conservation of energy.

However, if charges were to change the concentration or nature of traps in the phototransistor (photovoltaic effect), we know this can lead to a change in threshold voltage and a very large
EQE, that can be greater than 100%. In this case we are essentially photo-gating the TFT (i.e. light provides the role of an equivalent gate current). This phenomenon does not violate the conservation of energy because the TFT has gain, i.e. we are using external sources of energy to amplify the signal provided by light.

Question 5 [7 marks]:

a) Conventionally we use positive voltages to represent logic signals (low = 0V and high = +5V for example). Draw a diagram for a complementary inverter (i.e. an inverter comprising of separate p-type and n-type transistors) that works with negative voltages (e.g. low = 0V and high = -5V) and a negative supply voltage. Explain why this device would operate as expected.[4 marks]

This is a reasonably simple question if you think about it in terms of voltage transformations. Let’s first just look at a normal complementary inverter that uses positive voltages:

![Diagram of a normal complementary inverter](image)

Look at the voltage ranges applied to each terminal. I have labelled condition 1 as 0V in and +5V out, and condition 2 as +5V in and 0V out:

![Diagram showing voltage ranges](image)

Now consider transforming the voltage by -5V everywhere. As TFTs are only interested in voltages relative to each terminal (see ambipolar TFT lecture for example), we can expect exactly the same behavior from this inverter, just with the voltages transformed:

![Diagram showing transformed voltage ranges](image)
So, the same structure still reproduces the expected behavior where we have re-defined high and low signals to low = 0V and high = -5V. I.e. an input of -5V will provide an output of 0V, and an input of 0V will provide and output of -5V.

The only difference here is we now have -5V applied where the ground was, and ground where $V_{DD} = +5V$ was. Since it is conventional to put $V_{DD}$ at the top of the inverter and ground at the bottom, we should flip the structure to depict it properly:

Here the supply voltage is $V_{DD} = -5V$, as the question expects. Hence when using negative voltages, we can just flip the location of the p-type and n-type TFTs.

b) A complementary inverter is fabricated that has an infinite gain (i.e. perfectly sharp switching characteristics) at a switching voltage of $V_{in} = 3V$. If the inverter has the following voltage truth table, determine the low noise margin and high noise margin of this inverter. [3 marks]

<table>
<thead>
<tr>
<th>$V_{in}$</th>
<th>$V_{out}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0V to 3V</td>
<td>0.5V</td>
</tr>
<tr>
<td>3V to 5V</td>
<td>4V</td>
</tr>
</tbody>
</table>

Calculating noise margin involves swapping the x- and y-axes of the inverter curves and overlaying it with the original. Then the largest possible rectangle is drawn in each quadrant. Normally, to calculate noise margins of an inverter you would need to use an algorithm to maximize the area of the squares as it is not obvious by eye.

The one exception to this is if the inverter gain is $\infty$, in which case there is no ambiguity in the area of the overlapping curves, as they will always be perfect squares. The first thing we must do is plot the original input vs output voltage characteristics. We can just use the table above to do this.
Now we can flip the axes to see the overlap:

As the gain is infinite, the overlapping regions are perfect squares, hence we can draw them with no ambiguity (they are already drawn for us):

The lower square in voltage is the low (static) noise margin (SNM_L) and the higher square in voltage is the high static noise margin (SNM_H):

\[
\text{SNM}_L = 3V \\
\text{SNM}_H = 1V
\]
Question 6 [6 marks]:

a) Describe two structural problems that can occur when depositing semiconductors onto substrates with different coefficients of thermal expansion, at elevated temperatures.[2 marks]

If the semiconductor and the substrate do not have the same coefficient of thermal expansion (CTE) then cracking or bending can occur.

If a substrate is heated during semiconductor deposition it will expand. The semiconductor will then be deposited onto the substrate. As the substrate and the film cool back to room temperature, they will shrink. However, if their CTEs are not the same, then they will shrink by different amounts as they cool. In the strain is too high, this can either lead to the film cracking or, if the substrate is thin enough, bending an buckling.

b) An organic semiconductor that has a Young’s Modulus of 1.5 GPa is deposited over the entire surface of a small flexible RFID tag, which has dimensions of 5cm × 5cm when not stretched. The semiconductor is known to crack when a stress is above 4.5 GPa is applied. What length could the RFID tag be stretched to in one direction before the semiconductor cracks? Give your answer in cm.[2 marks]

This is basically a question testing the understanding of strain. We are told the Young’s modulus and the acceptable amount of strain, and need to determine the acceptable strain:

\[ Y = \frac{\sigma}{\varepsilon} \]
\[ \varepsilon = \frac{\sigma}{Y} \]

We are told the dimensions of the RFID tag are 5cm in each lateral dimension when not stretched, so whatever direction we stretch the tag in, we know that \( L_0 = 5\text{cm} \).

\[ \varepsilon = \frac{L_n - L_0}{L_0} \]

We are seeking the acceptable length when stretched \( (L_n) \):

\[ L_n - L_0 = \varepsilon L_0 \]
\[ L_n = \varepsilon L_0 + L_0 \]

Substituting strain from above:

\[ L_n = \frac{\sigma L_0}{Y} + L_0 \]

Now we can just enter numbers. Young’s modulus and stress both have units of pressure, so we can stick to cm for all the lengths:

\[ L_n = \frac{4.5 \times 5}{1.5} + 5 = 10\text{cm} \]
I.e. we can stretch the RFID tag to twice its original length.

c) Describe a possible use of a thermoelectric in flexible electronics.[1 marks]

A thermoelectric is a device which generates electricity from differences in heat. It can be used to power flexible electronic devices. A specific example is wearable electronics, where differences between body temperature and room temperature can act as the driver.

d) Provide a reason why you might want to use the compounds beta carotene in electronics.[1 mark]

In addition to being a semiconducting molecules, beta carotene is found in foods (carrots for example). For this reason it could be employed in bio-compatible or bio-degradable electronics.

Question 7 [5 marks]:

a) Briefly describe the operation of a chemiresistor.[1 mark]

A chemiresistor is a resistor that is simply a 2-terminal device that changes is resistance depending on the presence of certain chemical compounds. I.e. it is a chemical-sensitive resistor.

b) State the difference between a water-gated TFT and an organic electrochemical transistor.[1 mark]

In a water-gated TFT, ions in the solution are displaced by the applied gate field, which in-turn forms an electric double-layer at the interface between the solution and the semiconductor. This accumulation of ionic charge is what modulates the channel conductivity.

In an organic electrochemical transistor (OECT), ions in the solution also move under the influence of the applied gate field, however the distinction is, that in OECTs the ions cross the boundary into the transistor channel itself.

c) TFTs employing PEDOT:PSS as a channel material are called depletion-mode transistor. State what is meant by a depletion mode transistor.[1 mark]

A depletion mode transistor is simply a normally-on transistor. I.e. when no gate voltage is applied the channel is conducting, and to turn off the transistor a gate bias must be applied.

d) Describe, with diagrams, how an ion pump would be used in the human body.[2 marks]

Below is a very rough schematic of an ion pump.
By applying a bias between the reservoir of ions and the target, the ions can be controllably applied to the target by electrical signals.

When using applied to the human body, the target would be a particular region that periodically requires ion injection for treatment. The rest of the ion pump would be isolated, and not interact with the human body.