ECE / CHE 611 - Electronic Material Processing
Lecture 1: Introduction and Course Overview

Lecture 1
• Semiconductor Processing.
• Course Overview.
• Course Logistics.
• Regulations.
Semiconductor Processing

- The success of semiconductor technology has undoubtedly been one of humankind’s greatest achievements.
- We are incredibly lucky that the silicon has the properties it does, and is the 2nd most abundant element in earth’s crust.
- In 2019, transistors can be purchased at a cost of $10^{-7}$ USD / transistor when part of integrated circuit.
Why do you Care:

- Highly applicable knowledge for jobs in the semiconductor industry.
- The process we will cover is similar to the basic process followed by semiconductor fabrication facilities (e.g. Intel).
- The point of a course like this is to ensure you are able to go into an interview and talk with confidence on the subject.
- Information may also be useful / necessary for many aspects of your research.
- It is also an interesting subject (hopefully).

What is a Transistor?

- Fundamentally, when processing electronic materials we aim to make complex circuits from multiple transistors.
- A transistor is 3-terminal electronic switch.
- These are devices used to control the flow of current between two terminals via a third terminal.
- In this course we will not be discussing transistor operation, we will be looking at how they are made industrially.
Information Processing

- We use transistors to process information.

- The inverter (NOT gate) is the most simple circuit logic element.

Electronic Circuits

- Originally circuits were designed on a printed circuit board, with copper wires connecting components.
Logic Circuits

• Connecting multiple logic components together we are able to create complex circuits:

• This is a simple arithmetic logic unit (ALU):

1928: Transistor Patented

• Patent submitted in 1928 by Julius Edgar Lilienfeld.\[1\]

• Broadly similar to the metal-oxide-semiconductor field-effect transistors used today.

1947: The First Transistor

- Germanium was used in first transistor.
- Demonstrated by Bardeen Brattain Shockley in 1947.\(^1\)
- Working at Bell labs, NJ.

1958: First Integrated Circuit

- The first "integrated circuit" was developed in 1958.\(^1\)
- Jack Kilby, Texas Instruments.
- Multiple circuit elements on same piece of Germanium.
- This circuit was not monolithic.
- This circuit elements were isolated by cutting groves into the chip and connected with gold wires.

1960: First Monolithic IC

- The first monolithic planar integrated circuit was demonstrated in 1960.
  - By Robert Noyce at Fairchild Semiconductor.
  - He used silicon rather than germanium.
  - Since the intrinsic carrier concentration in silicon is so low ($n_i \sim 10^{10}$ cm$^{-3}$), isolated regions can be formed that are highly resistive.
  - p and n-regions could be formed by doping
  - It turns out that the native oxide silicon oxide is easy to grown and highly insulating.

MOSFETs

- Up to this point most IC’s were based on bipolar junction transistors (BJT’s). It was difficult to create a single chip with many (100’s) of transistors on it. The yield was very poor.
- Some at RCA (Radio Corporation of America) thought it would be possible to develop larger circuits from MOSFETs – based on the original Lilienfeld patent.

Bipolar Junction Transistor

Field-Effect Transistor (FET)
1965: First Stable MOSFETs

- Unfortunately silicon-based MOSFETs remained unstable and highly unpredictable.
- I.e. for a certain set of applied voltages, different currents were measured in different devices, and at different times.
- This was due to the quality of the SiO$_2$, and Si surface states.
- Individuals at RCA (Frederic Heiman, Steven Hofstein) and Andy Grove (Fairchild) eventually discovered that inclusion of sodium and hydrogen can overcome these issues.
- RCA demonstrated working MOSFET circuits in 1965.
- Andy Grove along with Gordon Moore founded Intel in 1968.

Integrated Circuits

- During the 1960’s and 1970’s more and more MOSFETs were combined into integrated circuits.
Integrated Circuits

- Original circuit design was painstaking and limited complexity.

Modern IC Development

- Nowadays the process is incredibly sophisticated.

Sand to Ingot  
Wafer Dicing
Modern IC Development

• Nowadays the process is incredibly sophisticated.

Photolithography

Ion Implantation

https://www.youtube.com/watch?v=d9SWNLZvA8g

Modern IC Development

• Nowadays the process is incredibly sophisticated.

Etching

Deposition

https://www.youtube.com/watch?v=d9SWNLZvA8g
Modern IC Development

- Nowadays the process is incredibly sophisticated.

Electrodeposition → CMP

https://www.youtube.com/watch?v=d95WvLZvA8y
Moore’s Law

• Suggested in the 1960’s by Intel’s founder Gordon Moore.
• The number of transistors that can inexpensively fit onto a single integrated circuit will double every 24 months.\[1\]
• Today transistors can be purchased at a cost of $10^{-7}$ USD / transistor when part of integrated circuit.

---

Moore’s Law

• Remarkably, it has held up for 40 years.

Moore’s Law

• This has been driven by reducing feature size:

Interconnects

22 nm Process

14 nm Process

80 nm minimum pitch

52 nm (0.65x) minimum pitch

52 nm Interconnect Pitch Provides
Better-than-normal Interconnect Scaling
Global Semiconductor Sales


Course Overview
**ECE 611**

- ECE 611 / CHE 611 is part of a series of graduate level courses on semiconductors and devices.

<table>
<thead>
<tr>
<th>Fall 2019</th>
<th>Winter 2020</th>
<th>Spring 2020</th>
</tr>
</thead>
<tbody>
<tr>
<td>ECE 611 / CHE 611</td>
<td>ECE 612 / CHE 612</td>
<td>ECE 613 / CHE 613</td>
</tr>
</tbody>
</table>

**Material Processing**
- Silicon growth.
- Processing.
- Layer Deposition.

**Process Integration**
- VLSI.
- Interconnects.
- Multilayer technology.

**Materials Characterization**
- Electronic, optical, structural, chemical properties.

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**ECE 611**

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<table>
<thead>
<tr>
<th>Fall 2020</th>
<th>Winter 2021</th>
<th>Spring 2021</th>
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</thead>
<tbody>
<tr>
<td>ECE 614</td>
<td>ECE 615</td>
<td>ECE 616</td>
</tr>
</tbody>
</table>

**Semiconductors**
- Energy bands.
- Carrier statistics.
- Transport.

**2 Terminal Devices**
- Diodes.
- Capacitors.
- Schottky Contacts.
- Heterojunctions.

**3 Terminal Devices**
- Bipolar junction transistors.
- Field-effect transistors.
ECE 611 vs ECE 418 / 518

• There is some overlap with the lab based class ECE 418 / 518:

418 / 518
- Safety, Cleanrooms, Cleaning
- Capacitor Operation
- Transistor Operation
- Laboratory hands-on experience
- Electrical measurement and testing
- Silicon Growth & Properties
- Vacuum Science
- Oxidation
- Diffusion
- Basic Photolithography
- Ion Implantation
- Thin Film Growth
- Electrochemical Deposition of Metals
- Plasmas
- Modeling with Athina / Atlas
- Chemical Vapor Deposition
- Advanced Photolithography
- Future of Electronics

611
- These subjects will be covered in more depth in ECE / CHE 611
- This was taught in ECE 418/518 last year, but will be removed in the future

Basic Properties of Silicon

https://youtu.be/ApqFLVd0XaI?t=9m10s
Growth of Crystalline Silicon

Vacuum Science
**Electrochemical Deposition**

Electrolyte solution

Electrode

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Fall 2019 - John Labram

**Plasmas**

Power Supply

Switch

Ion

Electron

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Fall 2019 - John Labram
Oxidation

Diffusion
Ion Implantation

- Beam of ions
- X-scan
- Y-scan
- Implant disk
- Fixed ion beam
- Si Wafer

Athena Modeling
**Chemical Vapor Deposition**

1. Bulk transport
   - Carrier gas (to maintain high pressure & slow reaction rate)

2. Transport across boundary layer

3. Adsorption

4. Surface diffusion

5. Decomposition

6. Reaction with film

7. Diffusion of gaseous by-product

8. Bulk transport of by product

\[
J_1 \propto D g \Delta C
\]

\[
J_2 \propto k_i C_i
\]

**Thin Film Growth**

- Atom arrives:
- Migration:
- Collison and Combination:
- Nucleation:
- Coalescence:
- Continuity:
Basic Photolithography

- Strip
- Etch
- Develop
- Expose

Advanced Photolithography

- Mask
- Condenser
- Mirrors
- Wafer
- Plasma

Extreme ultraviolet lithography

SiO₂

40 nm

44/77
Etching

Substrate: Si

SiO₂

Photoresist

Solution of reactants

Wafers

Future of Electronics

Course Logistics

Instructor

- John Labram.
- Assistant Professor, Electrical Engineering and Computer Science.
- Office Location: 3103 Kelley Engineering Center.
- Office Hours: Monday 13:00 – 14:00.
- Email: john.labram@oregonstate.edu.
- Website: http://eecs.oregonstate.edu/people/Labram-John.
Lectures

- The lectures are compulsory to attend.
- There will be two 80 minute slots per week:
  - Tuesday: 10:00 am – 11:20 am.
  - Thursday: 10:00 am – 11:20 am.
- Lectures will take place in 124 Kearney Hall.

Lectures

- The PowerPoint slides will be provided online after each lecture.
  - [http://classes.engr.oregonstate.edu/eecs/fall2019/ece611/lectures.html](http://classes.engr.oregonstate.edu/eecs/fall2019/ece611/lectures.html)
- I will also provide a hard copy for each of you at the start of the lecture.
  - It will be helpful to make notes on the slides of any extra / contextual information that is not written down.
- Some lectures will contain examples, but homeworks and the book will serve as the best place to practice.
Textbook

- The content of the course is based on this book.
- We will also cover a few other topics not in the book.

Course Website

- The course website can be found:
  - [http://classes.engr.oregonstate.edu/eecs/fall2019/ece611/index.html](http://classes.engr.oregonstate.edu/eecs/fall2019/ece611/index.html).
- Homeworks, solutions, lecture slides, details for the term paper, and general information will be located here.
- This should be the first place you look for course information.
### Lecture Schedule

- This is a preliminary schedule – is subject to change.

<table>
<thead>
<tr>
<th>Week</th>
<th>Day</th>
<th>Date</th>
<th>Month</th>
<th>Lecture</th>
<th>Topic</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Thur</td>
<td>26</td>
<td>Sep</td>
<td>1</td>
<td>Introduction</td>
</tr>
<tr>
<td>1</td>
<td>Tue</td>
<td>1</td>
<td>Oct</td>
<td>2</td>
<td>Silicon Properties and Growth</td>
</tr>
<tr>
<td>1</td>
<td>Thur</td>
<td>3</td>
<td>Oct</td>
<td>3</td>
<td>Vacuum Science and Technology</td>
</tr>
<tr>
<td>2</td>
<td>Tue</td>
<td>8</td>
<td>Oct</td>
<td>4</td>
<td>Electrochemical Deposition of Metals</td>
</tr>
<tr>
<td>2</td>
<td>Thur</td>
<td>10</td>
<td>Oct</td>
<td>5</td>
<td>Plasmas</td>
</tr>
<tr>
<td>3</td>
<td>Tue</td>
<td>15</td>
<td>Oct</td>
<td>6</td>
<td>Oxidation</td>
</tr>
<tr>
<td>3</td>
<td>Thur</td>
<td>17</td>
<td>Oct</td>
<td>7</td>
<td>Diffusion</td>
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<tr>
<td>4</td>
<td>Tue</td>
<td>22</td>
<td>Oct</td>
<td>8</td>
<td>Ion Implantation</td>
</tr>
<tr>
<td>4</td>
<td>Thur</td>
<td>24</td>
<td>Oct</td>
<td></td>
<td>No Lecture - Preparation for Midterm</td>
</tr>
<tr>
<td>5</td>
<td>Tue</td>
<td>29</td>
<td>Oct</td>
<td></td>
<td>Midterm</td>
</tr>
<tr>
<td>5</td>
<td>Thur</td>
<td>31</td>
<td>Oct</td>
<td>9</td>
<td>Modeling with Athina 1</td>
</tr>
<tr>
<td>6</td>
<td>Tue</td>
<td>5</td>
<td>Nov</td>
<td>10</td>
<td>Modeling with Athina 2</td>
</tr>
<tr>
<td>6</td>
<td>Thur</td>
<td>7</td>
<td>Nov</td>
<td>11</td>
<td>CVD</td>
</tr>
<tr>
<td>7</td>
<td>Tue</td>
<td>12</td>
<td>Nov</td>
<td>12</td>
<td>Thin Film Growth</td>
</tr>
<tr>
<td>7</td>
<td>Thur</td>
<td>14</td>
<td>Nov</td>
<td>13</td>
<td>Basic Photolithography</td>
</tr>
<tr>
<td>8</td>
<td>Tue</td>
<td>19</td>
<td>Nov</td>
<td>14</td>
<td>Advanced Photolithography</td>
</tr>
<tr>
<td>8</td>
<td>Thur</td>
<td>21</td>
<td>Nov</td>
<td>15</td>
<td>Etching</td>
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<tr>
<td>9</td>
<td>Tue</td>
<td>26</td>
<td>Nov</td>
<td>16</td>
<td>The Future of Electronics</td>
</tr>
<tr>
<td>9</td>
<td>Thur</td>
<td>28</td>
<td>Nov</td>
<td></td>
<td>No Lecture - Thanksgiving</td>
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<tr>
<td>10</td>
<td>Tue</td>
<td>3</td>
<td>Dec</td>
<td></td>
<td>No Lecture - John at Conference</td>
</tr>
<tr>
<td>10</td>
<td>Thur</td>
<td>5</td>
<td>Dec</td>
<td></td>
<td>No Lecture - John at Conference</td>
</tr>
<tr>
<td></td>
<td>Fri</td>
<td>13</td>
<td>Dec</td>
<td></td>
<td>Final Exam</td>
</tr>
</tbody>
</table>

### Assessment

- The final grade will consist of the following contributions:

<table>
<thead>
<tr>
<th>Assessment</th>
<th>Percentage of Final Grade</th>
</tr>
</thead>
<tbody>
<tr>
<td>Homework</td>
<td>40</td>
</tr>
<tr>
<td>Mid-Term Exam</td>
<td>20</td>
</tr>
<tr>
<td>Term Paper</td>
<td>20</td>
</tr>
<tr>
<td>Final Exam</td>
<td>20</td>
</tr>
</tbody>
</table>
Homework

- There will be a total of 4 homeworks.
- Each homework carries equal weight.
- The homeworks are designed to test your understanding of the concepts covered in the lectures.
  - Sometimes you will be expected to apply knowledge obtained in the lectures to new (previously unseen) situations.
- The homeworks overall contribute 40% of the course grade.
  - 10% each.

Homework

- The homework will be a combination of:
  - **Text-based answers.** I.e. you will be expected to describe a process or phenomenon in words.
  - **Analytical problems.** Derivations and/or calculations that can be solved with just pen, paper, and calculator.
  - **Data analysis.** You will be provided with some simple numerical data and expected to process it to extract parameters / draw conclusions.
  - **Simulations.** You will use Athena / Atlas to simulate growth of electronic materials.
Homework

• The homework schedule is as follows:

<table>
<thead>
<tr>
<th>Homework #</th>
<th>Set</th>
<th>Due</th>
<th>Returned</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Tuesday 10/08/19</td>
<td>Tuesday 10/15/19</td>
<td>Tuesday 10/22/19</td>
</tr>
<tr>
<td>2</td>
<td>Tuesday 10/22/19</td>
<td>Tuesday 10/29/19</td>
<td>Tuesday 11/05/19</td>
</tr>
<tr>
<td>3</td>
<td>Tuesday 11/05/19</td>
<td>Tuesday 11/12/19</td>
<td>Tuesday 11/19/19</td>
</tr>
<tr>
<td>4</td>
<td>Tuesday 11/19/19</td>
<td>Tuesday 11/26/19</td>
<td>Friday 12/13/19</td>
</tr>
</tbody>
</table>

Homework

• Please hand in homework at the start of the lecture on the due date.
  • Please make your name and OSU ID clearly visible.
  • Please circle / make a box around the final answer if applicable.
• Late homework will be deducted 10% per day late for a maximum of 5 days, after which the homework grade will be zero.
  • E.g. if you scored 85% on a homework, but you hand it in 2 days late, you will receive a grade of 65%.
Modeling

- After the midterm we will spend two lectures looking at Athena and Atlas. These are packages we can use to simulate the properties of silicon wafers as a function of various processing conditions.
- For example it allows you to calculate impurity concentrations, layer thickness, and much more for processes such as oxidation, diffusion, implantation and deposition for temperature.
- Athena is the Silvaco version of SUPREM (Stanford University PRocess Engineering Module)
- More details will be made available in the future...

Term Paper

- As part of this course you will be expected to write a term paper based on a modern topic related to electronic materials processing.
- This can be viewed as a mini literature review.
- The paper will be 4 – 5 pages (excluding references).
- It will contribute 20% of the grade for the class.
- You will be given a choice of topics on October 29th, and be expected to provide a ranked list of your top 5 topics by 5pm on Friday November 1st.
- The due date for the term paper is Tuesday November 19th.
Examinations

- There will be two examinations: one midterm, one final.
- They will carry equal weight to the final course grade: 20% each.
- The midterm will examine content covered in Lectures 1-8 (inclusive).
- The final will examine content covered in Lectures 9-16 (inclusive).
- The exams will consist of optional questions. For example, you may be expected to complete 2 out of 3 questions.

Examinations

- The exams are designed to test your ability to apply knowledge acquired during the lectures to new situations.
- Both exams will be closed book and closed notes.
- Besides a small number of well-known equations, most equations will be provided at the start of the exam.
- All physical constants and parameters will also be provided.
- You will be allowed (and expected) to use a calculator.
Equations

- You will be given most equations. However, simple relationships you would be expected to know. E.g.
  - Density:
    \[ n_{2D} = \frac{1}{A} \quad n_{3D} = \frac{1}{V} \]
  - Area:
    \[ A = \pi r^2 \]
  - Surface area of sphere:
    \[ A = 4\pi r^2 \]

Equations

- You will be given most equations. However, simple relationships you would be expected to know. E.g.
  - Chain rule:
    \[ \frac{df}{dx} = \frac{df}{dg} \frac{dg}{dx} \]
  - Standard derivatives:
    \[ \frac{d}{dx} (ae^{bx}) = abe^{bx} \quad \frac{d}{dx} (\ln(ax)) = \frac{1}{x} \]
    \[ \frac{d}{dx} (\sin(ax + b)) = -a \cdot \cos(ax + b) \]
    \[ \frac{d}{dx} (\cos(ax + b)) = -a \cdot \sin(ax + b) \]
Equations

- You will be given most equations. However, simple relationships you would be expected to know. E.g.

- Velocity:
  \[ v = \frac{x}{t} \]

- Current from charge:
  \[ I = \frac{Q}{t} \]

- Ohm’s Law:
  \[ V = IR \]

- Kinetic Energy:
  \[ E = \frac{1}{2}mv^2 \]

- Momentum:
  \[ p = mv \]

- Mass density:
  \[ \rho = \frac{m}{V} \]

Equations

- Limits of exponentials:
  \[ e^0 = 1 \]
  \[ e^{-\infty} = 0 \]
  \[ e^{\pm1/\infty} = e^0 = 1 \]

- Unit conversions
  \[ 1\text{Å} = 10^{-10}\text{m} \]
  \[ 1\text{μm} = 10^{-6}\text{m} \]
  etc ...

Lecture 1 – Thursday September 26th 2019
Exam Style Example

- All constants will be provided.
- All relevant formulae will also be provided.
- Parameters will be labeled as clearly as possible.

\[ P = \frac{nkT}{V} \]

**Molar Gas Law:**

- \( P \) is the gas pressure.
- \( n \) is the number density of gas molecules.
- \( k \) is the Boltzmann Constant.
- \( T \) is the gas temperature.

**Molecular Velocity:**

\[ \frac{\sqrt{8RT}}{\sqrt{\pi m}} \]

- \( \sqrt{\frac{8RT}{\pi m}} \) is the maximum velocity of the molecule.
- \( \sqrt{\frac{8RT}{\pi m}} \) is the root mean square velocity.

**Exam Schedule:**

- The exams will take place in Kearney Hall 124.
- The exams will last 80 minutes.
  - Please ensure you arrive on time so the lectures can begin promptly.
- The below schedule is provisional and subject to change:

<table>
<thead>
<tr>
<th>Exam</th>
<th>Week</th>
<th>Date</th>
<th>Time</th>
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<tbody>
<tr>
<td>Midterm</td>
<td>5</td>
<td>Tuesday 10/29/19</td>
<td>10:00 am</td>
</tr>
<tr>
<td>Final</td>
<td>F</td>
<td>Friday 12/13/19</td>
<td>09:30 am</td>
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Grading

- Grade boundaries are as follows:

<table>
<thead>
<tr>
<th>Lower Bound (%)</th>
<th>Upper Bound (%)</th>
<th>Grade</th>
</tr>
</thead>
<tbody>
<tr>
<td>93</td>
<td>100</td>
<td>A</td>
</tr>
<tr>
<td>90</td>
<td>92</td>
<td>A-</td>
</tr>
<tr>
<td>87</td>
<td>89</td>
<td>B+</td>
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<tr>
<td>83</td>
<td>86</td>
<td>B</td>
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<tr>
<td>80</td>
<td>82</td>
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<td>C-</td>
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<tr>
<td>67</td>
<td>69</td>
<td>D+</td>
</tr>
<tr>
<td>63</td>
<td>66</td>
<td>D</td>
</tr>
</tbody>
</table>

- Percentages will be rounded-off to the nearest whole percent to determine letter grade

Grading

- Hopefully I will not have to curve.
- But it depends on results.
- I may try to ~match grade distributions from previous years.
- But can go up and down depending on absolute performance.
Regulations

Cheating and Student Conduct

• Academic dishonesty is defined as an intentional act of deception in one of the following areas:
  • **Cheating**- use or attempted use of unauthorized materials, information or study aids.
  • **Fabrication**- falsification or invention of any information.
  • **Assisting**- helping another commit an act of academic dishonesty.
  • **Tampering**- helping another commit an act of academic dishonesty.
  • **Plagiarism**- representing the words or ideas of another person as one's own.
Cheating and Student Conduct

• When evidence of academic dishonesty comes to the instructor's attention, the instructor will document the incident, permit the accused student to provide an explanation, advise the student of possible penalties, and take action.
• The instructor may impose any academic penalty up to and including an "F" grade in the course after consulting with his or her department chair and informing the student of the action taken.

Disruptive Behavior

• While the University is a place where the free exchange of ideas and concepts allows for debate and disagreement, all classroom behavior and discourse should reflect the values of respect and civility.
• Behaviors which are disruptive to the learning environment will not be tolerated.
• As your instructors, we are dedicated to establishing a learning environment that promotes diversity of race, culture, gender, sexual orientation, and physical disability.
Disruptive Behavior

- Anyone noticing discriminatory behavior in this class, or feeling discriminated against should bring it to the attention of the instructors or other University personnel as appropriate.

Summary

- We have introduced the subject of electronics material processing, and why it is important.
- We have covered the course content.
- We also covered some of the logistical / organizational aspects of the course.
Next Time...

- Basic properties of silicon.

https://youtu.be/ApqFLVd0XaI?t=9m10s