ECE 617 – Thin Film Electronics
Fall 2020
Homework 7
Due Monday November 16th at 2:00pm

Question 1 [3 marks]:
a) Consider an ambipolar TFT which has a threshold voltage for electrons of $V_{Te} = +7.5$ V and a threshold voltage for holes of $V_{Th} = -10$ V. If you apply a gate voltage of $V_G = +25$ V, state the range of drain voltages you would have to apply to the TFT to observe that the electron channel is saturated but there are no holes in the channel (i.e. the drain voltage required to observe conventional unipolar saturation regime)?[3 marks]

Question 2 [7 marks]:
a) Figure 1 below shows a bilayer ambipolar TFT with a p-type semiconductor deposited onto a separate n-type semiconductor. Because bilayer TFT are not prevented from saturating in the same way as a single-layer ambipolar TFT are, they can be viewed as two TFTs in parallel. For this reason the standard gradual channel approximation can be employed. The TFT has dimensions of $W = 1$ mm and $L = 100$ μm. If we apply gate and drain voltages of $V_G = +10$ V, and $V_D = +50$ V, use the parameters in the table below to determine the source drain current in this ambipolar bilayer TFT.[7 marks]

<table>
<thead>
<tr>
<th></th>
<th>SiO$_2$</th>
<th>N-Type</th>
<th>P-Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric Constant, $\kappa$</td>
<td>3.9</td>
<td>16</td>
<td>3</td>
</tr>
<tr>
<td>Carrier Mobility (cm$^2$/Vs)</td>
<td>NA</td>
<td>10</td>
<td>0.1</td>
</tr>
<tr>
<td>Layer Thickness (nm)</td>
<td>200</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>Threshold Voltage (V)</td>
<td>NA</td>
<td>+5</td>
<td>0</td>
</tr>
</tbody>
</table>

Figure 1 Schematic (side-view) diagram of bilayer ambipolar TFT. The top semiconducting layer is able to transport holes only, the bottom semiconducting layer is able to transport electrons only.

Hint: the two following equations will be useful:
Capacitance of Capacitors in Series:

\[ C_T = \frac{1}{\frac{1}{C_1} + \frac{1}{C_2} + \cdots + \frac{1}{C_n}} \]

- \( C_T \) is the total capacitance of the capacitors in series.
- \( C_1, C_2, \ldots, C_n \) is the capacitance of the individual capacitors in series.

Capacitance per Unit Area of Parallel Plate Capacitor:

\[ C = \frac{\varepsilon_0 \kappa}{d} \]

- \( C \) is the capacitance per unit area (e.g. F/cm²).
- \( \varepsilon_0 \) is the vacuum permittivity.
- \( \kappa \) is the relative permittivity (dielectric constant).
- \( d \) is the separation distance of the plates.

**Question 3 [10 marks]:**

a) Figure 2 shows a schematic of a single-layer ambipolar TFT biased at \( V_G = +10V \) and \( V_D = +30V \). At these voltages the TFT is observed to emit light at a distance \( x_0 \) from the source electrode. Such a TFT can be viewed as two unipolar TFTs in series. By assuming that the recombination rate of holes and electrons are infinite at \( x = x_0 \), use the Smits model to determine \( x_0 \) at \( T = 300K \). The relevant parameters for this TFT at 300K are listed in the below table. Assume the threshold voltage for holes and electrons are equal and zero: \( V_{T_e} = V_{T_h} = V_T = 0 \), and the channel length is \( L = 50\mu m \). [10 marks]

\[
\begin{array}{|c|c|c|}
\hline
\text{Parameter} & \text{Electrons} & \text{Holes} \\
\hline
\gamma (A) & 3.7 \times 10^{13} & 1.7 \times 10^{15} \\
T_0 (K) & 465 & 443 \\
\hline
\end{array}
\]

**Figure 2** Schematic (side-view) diagram of light-emitting ambipolar TFT. The position of recombination is defined as \( x = x_0 \) here. The applied gate voltage is \( V_G = +10V \), the applied drain voltage is \( V_D = +30V \). The channel length is \( L = 50\mu m \).

**Hint 1:** You will need to enforce the condition that source-drain current is constant throughout the channel.
Hint 2: Be careful when defining the effective drain voltage in your two channels. The n-type channel is saturated (pinched off) at $x_0$. Hence you can say for the n-channel that the effective $V_D = V_G$ at $x = x_0$.

Hint 3: For carriers flowing from the drain (i.e. backwards) remember to transform voltages.

Hint 4: Defining the following parameter will be helpful:

$$C = \frac{\gamma_h T_{0e} (2T_{0e} - T)}{\gamma_e T_{0h} (2T_{0h} - T)}$$

For reference, the two relevant equations are below:

**Smits Model for n-type TFT:**

$$I_D = \gamma_e \frac{W}{L} \frac{T}{2T_{0e}} \frac{T}{2T_{0e} - T} \left[ (V_G - V_T)^{2T_{0e}/T} - (V_T - V_G - V_D)^{2T_{0h}/T} \right]$$

- $I_D$ is the source-drain current.
- $\gamma_e$ is the gamma parameter for electrons in this semiconductor.
- $W$ is the transistor channel width.
- $L$ is the transistor channel length.
- $T$ is the temperature.
- $T_{0e}$ is the characteristic temperature describing the width of electron states of this semiconductor.
- $V_G$ is the applied gate voltage.
- $V_T$ is the threshold voltage.
- $V_D$ is the applied drain voltage.

**Smits Model for p-type TFT:**

$$I_D = \gamma_h \frac{W}{L} \frac{T}{2T_{0h}} \frac{T}{2T_{0h} - T} \left[ (V_T - V_G)^{2T_{0h}/T} - (V_T - V_G + V_D)^{2T_{0h}/T} \right]$$

- $I_D$ is the source-drain current.
- $\gamma_h$ is the gamma parameter for holes in this semiconductor.
- $W$ is the transistor channel width.
- $L$ is the transistor channel length.
- $T$ is the temperature.
- $T_{0h}$ is the characteristic temperature describing the width of hole states of this semiconductor.
- $V_G$ is the applied gate voltage.
- $V_T$ is the threshold voltage.
- $V_D$ is the applied drain voltage.