Question 1 [15 marks]:

a) Conventionally we use positive voltages to represent logic signals (low = 0V and high = +5V for example). Draw a diagram for a complementary inverter (i.e. an inverter comprising of separate p-type and n-type transistors) that works with negative voltages (e.g. low = 0V and high = -5V) and a negative supply voltage. Explain why this device would operate as expected.[3 marks]

This is a reasonably simple question if you think about it in terms of voltage transformations. Let’s first just look at a normal complementary inverter that uses positive voltages:

![Diagram of a normal complementary inverter](image)

Look at the voltage ranges applied to each terminal. I have labelled condition 1 as 0V in and +5V out, and condition 2 as +5V in and 0V out:

![Voltage ranges](image)

Now consider transforming the voltage by -5V everywhere. As TFTs are only interested in voltages relative to each terminal (see ambipolar TFT lecture for example), we can expect exactly the same behavior from this inverter, just with the voltages transformed:
So, the same structure still reproduces the expected behavior where we have re-defined high and low signals to low = 0V and high = -5V. I.e. an input of -5V will provide an output of 0V, and an input of 0V will provide an output of -5V.

The only difference here is we now have -5V applied where the ground was, and ground where \( V_{DD} = +5V \) was. Since it is conventional to put \( V_{DD} \) at the top of the inverter and ground at the bottom, we should flip the structure to depict it properly:

Here the supply voltage is \( V_{DD} = -5V \), as the question expects. Hence when using negative voltages, we can just flip the location of the p-type and n-type TFTs.

b) A complementary inverter is fabricated that has an infinite gain (i.e. perfectly sharp switching characteristics) at a switching voltage of \( V_{in} = 3V \). If the inverter has the following voltage truth table, determine the low noise margin and high noise margin of this inverter. [3 marks]

<table>
<thead>
<tr>
<th>( V_{in} )</th>
<th>( V_{out} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0V to 3V</td>
<td>0.5V</td>
</tr>
<tr>
<td>3V to 5V</td>
<td>4V</td>
</tr>
</tbody>
</table>

Calculating noise margin involves swapping the \( x \)- and \( y \)-axes of the inverter curves and overlaying it with the original. Then the largest possible rectangle is drawn in each quadrant. Normally, to calculate noise margins of an inverter you would need to use an algorithm to maximize the area of the squares as it is not obvious by eye.

The one exception to this is if the inverter gain is \( \infty \), in which case there is no ambiguity in the area of the overlapping curves, as they will always be perfect squares. The first thing we must
do is plot the original input vs output voltage characteristics. We can just use the table above to do this.

![Graph](image1)

Now we can flip the axes to see the overlap:

![Graph](image2)

As the gain is infinite, the overlapping regions are perfect squares, hence we can draw them with no ambiguity (they are already drawn for us):

![Graph](image3)

The lower square in voltage is the low (static) noise margin (SNM_L) and the higher square in voltage is the high static noise margin (SNM_H):

\[
\text{SNM}_L = 2.5V \\
\text{SNM}_H = 1V
\]
c) Figure 2 shows the output voltage as a function of input voltage for a highly-optimized complementary inverter. This data is available to download [here](#) with input voltage step sizes of 100 mV and [here](#) with input voltage step sizes of 10mV. Determine the gain for this inverter from both sets of data, and use the result as an example to explain why care should be taken when measuring inverters to report gain. [5 marks]

To evaluate the gain \( g \) of an inverter you need to take the first derivative of output voltage with respect to input voltage:

\[
g = \left| \frac{dV_{out}}{dV_{in}} \right|
\]

This is plotted as a function of gate voltage for the two data sets below:
From this data we see that the peak gain is \( 18.3 \) if we measure with 100 mV voltage step size, and \( 23.9 \) if we measure with 10 mV step size. The point here is that if the step size is too small, we can under-estimate the peak gain. This due to the fact that we are carrying out numerical differentiation rather than actual differentiation:

\[
\frac{\Delta V_{\text{out}}}{\Delta V_{\text{in}}} \neq \frac{dV_{\text{out}}}{dV_{\text{in}}}
\]

d) State one positive aspect of using ambipolar TFTs in inverters for thin film electronics.[1 mark]

We can use the same material as both the p-type and n-type component in complementary inverters. This potentially simplifies the semiconductor deposition process greatly, which could in turn save cost.

c) State one negative aspect of using ambipolar TFTs in inverters for thin film electronics.[1 mark]

Because ambipolar devices never completely turn off, the output on- and off-states are less well defined in complementary-like ambipolar inverters. For this reason the noise-margins are likely to be lower than pure complementary (separate p-type and n-type TFTs) inverters.

d) Figure 2 below shows a circuit made from p-type and n-type TFTs. Assuming the static noise margins are high in this circuit, sketch the output voltage as a function of time, with a positive supply voltage. The qualitative form of the output is important, not the absolute numbers.[2 marks]

![Circuit diagram]

Figure 2 Circuit made from a combination of p-type and n-type TFTs.

This is a ring oscillator. If each inverter stage operates as expected, the output voltage should oscillate between the high and low voltage output of the last stage in the oscillator.
Question 1 [5 marks]:

a) Provide an example of a printable electronic device that could conceivably require non-volatile memory onboard.[1 mark]

There are many potential answers to this question. Examples we talked in class are below:
- Electronic food packaging that tracks temperature with time.
- Unique identifiers that have information about an object written into them.

Any other reasonable answer.

b) Provide a reason why it might be challenging to replicate flash memory, identically, using thin film electronics.[1 mark]

The main reason is that flash memory uses a floating gate and a very thin tunneling dielectric. It is likely that making very thin (< 5 nm) layers which are both uniform and pinhole free, is going to be very challenging with scalable large area techniques (e.g. printing, sputtering).

c) Explain briefly why it is desirable in three terminal memory devices for memory states to be defined by modifying the threshold voltage, as opposed to say changing the average mobility.[1 mark]

By modifying the threshold voltage by only a few volts you can change the measured source drain current by many orders of magnitude for certain values of $V_G$ and $V_D$. This means, if done correctly, you have very well defined on and off states.

Even if you were able to controllably change the average mobility by a factor of 10 (a challenging thing to do), you would only modulate the conductance of on and off states by the same ratio.

d) Briefly explain why you would expect redox based memory devices to have long write and erase times.[1 mark]

Redox memory devices rely upon moving a compound or element toward another, then waiting for a reaction to occur, before the state can be written or erased. This is a process which takes a long time.

e) Briefly explain why you would expect filamentary conduction to have a long retention time.[1 mark]

Filamentary conduction relies upon physical movement of material inside of the device. It is hence likely that once in place, the state will be very stable.