Micro-Power Data Converters

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Outline

• Micro-power D/A converters:
  - Overview of CMOS DACs
  - Switched-capacitor DACs
  - Quasi-passive two-C DAC
  - Quasi-passive pipeline DAC
  - Delta-sigma DACs.

• Micro-power A/D converters:
  - Overview of CMOS ADCs
  - SAR ADC, pipeline SAR ADC
  - Multiplexed incremental ADC
  - Extended-count hybrid ADC.
Applications

- Battery-powered medical devices (hearing aids, ECG, EEG, etc. sensors, brain stimulators);
- Wireless sensor networks for industrial and environmental applications;
- RFID systems.

Typical target specifications:

- DACs: BW up to 20 kHz, ENOB 14 - 15 bits, 20-bit input;
- ADCs: BW = up to 5 kHz; ENOB > 12 bits; power < 5 microwatts; input signal amplitude 0.1 ~ 5 mV.
Power Saving in Data Converters

- Stages: S/Hs, buffers, comparators, SC blocks.
- S/H: whenever possible, use passive (SC) circuitry; if not, use direct charge transfer (DCT) amplifier stage.
- Buffers: use DCT stage.
- Comparators: use dynamic circuitry.
- SC circuits: use minimally busy circuitry. Reduce dynamic power dissipation.
- Transistor circuits: consider weak inversion operation.
- Logic: consider asynchronous switching.
Classification of DACs

• “Nyquist-rate” DAC: memoryless, one-to-one correspondence between input digital word and output analog sample;

• “Oversampled” DAC: has memory (finite or infinite length), so digital output depends on all previous inputs and outputs.

• Sampling rates may not be very different.
## Classification of Nyquist-rate DACs

Classification of Nyquist-rate D/A converters

$(T=$clock period, $N=$resolution in bits)

<table>
<thead>
<tr>
<th>Algorithm</th>
<th>Conversion time</th>
<th>Latency (delay)</th>
<th>Resolution (typical)</th>
<th>Usual implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parallel (flash)</td>
<td>$T$</td>
<td>$T$</td>
<td>5-12 bits</td>
<td>Current steering; voltage division; charge sharing</td>
</tr>
<tr>
<td>Pipeline</td>
<td>$T$</td>
<td>$NT$</td>
<td>8-12 bits</td>
<td>Passive SC; active (opamp) stages</td>
</tr>
<tr>
<td>Serial</td>
<td>$NT$</td>
<td>$NT$</td>
<td>8-12 bits</td>
<td>2-capacitor SC stage</td>
</tr>
<tr>
<td>Counting</td>
<td>$2^NT$</td>
<td>$2^NT$</td>
<td>15-22 bits</td>
<td>SC integrator + digital comparator</td>
</tr>
</tbody>
</table>
Nyquist-Rate DACs

- Parallel (flash) DACs: conversion time and latency is $T$; resolution $N < 10$ bits; implementation R-string or R-2R ladder, current sources, switched-capacitor (SC) stage.

- Pipelined DACs: conversion time $T$; latency $NT$; $N < 14$ bits; SC stages.

- Serial DACs: conversion time and latency $NT$; $N < 12$ bits; 2-C stages.

- Counting DAC: conversion time and latency $= 2^N \cdot T$; $N < 24$ bits; SC or RC integrators.
Oversampled CMOS DACs

- Nyquist-rate vs. oversampled DACs: in oversampled DAC, the word length can be reduced to 1 ~ 5 bits.

- Mismatch errors can be suppressed in signal band using dynamic element matching.

- High accuracy can be obtained with simple low-power analog circuitry, but complex digital delta-sigma loop and prefilter are required.

- May only be economical for high-resolution low-power DAC applications.
Nyquist-Rate Parallel DACs

- R-string or R-2R ladder: large area, large mismatch errors, static dissipation – seldom practical in low-power applications.

- Current-source DAC: large mismatch error, static dissipation – seldom used in slow low-power DACs.

- SC stages: binary-weighted or unary (unit-element-based) charge redistribution circuits. Unary is more complex, but the glitches are reduced, the monotonicity is guaranteed, and dynamic element matching may be possible.
SC DAC Stages

- Unary SC DAC: monotonic, low glitch.
SC DAC Stages

• Binary SC DAC: non-monotonic, large glitch.

• Both circuits use correlated double sampling for amplifier offset cancellation and for gain boosting.
SC DAC Using DCT Circuit

- Direct charge transfer (DCT) reduces the slewing and settling requirements on the amplifier, since it need not provide current to the feedback branch:
Two-Capacitor DAC

• Simple and fast, but mismatch introduces large spurs.
• Digital dither, correction or mismatch shaping possible.
• Serial DAC; needs $N$ clock periods for $N$-bit resolution.
• May be time interleaved for Nyquist-rate operation.
Quasi-Passive Cyclic DAC

- Operation for $x(n) = 1, 0, 1, 1$:
  - Charge redistribution between two equal-valued capacitors
  - Serial digital input; LSB first
  - $\Phi_1$ and $\Phi_2$ are two non-overlapping clock phases
  - Conversion follows equation
    $$V_{\text{out}} = V_{\text{ref}} \sum_{i=1}^{N} b_i 2^{-i}$$

Capacitor Mismatch

- Capacitor mismatch effects
  - Conversion accuracy limited by capacitor matching accuracy;
  - Capacitor mismatch introduces nonlinearity;
  - Plots show performance degradation (bottom) in SNDR and SFDR compared with output spectrum from DAC with ideal matching (top)

Matched 12-b
- SNDR = 73.8 dB
- SFDR = 98.2 dB

1% Mismatch 12-b
- SNDR = 51.6 dB
- SFDR = 54.3 dB
Mismatch Compensation (1)

- Switching techniques:
  - Compensative switching
    - The roles of the two capacitor is interchangeable
    - The roles of the capacitors can be chosen for every bit
    - An algorithm was developed to minimize the conversion error for any digital word
    - The switching pattern is input dependent
    - First-order error canceled for 31% of the input codes; reduced to 1/10 for 48% of the input codes.

Mismatch Compensation (2)

- Switching techniques:
  - Complementary switching:
    - Digital word fed to DAC twice; once with normal arrangement, once with swapped roles of $C_1$ and $C_2$
    - Outputs of the two conversions are added (or averaged), actively or passively;
    - First-order mismatch compensation, at cost of doubled conversion time.

Mismatch Compensation (3)

• Switching techniques:
  – Input-word-splitting compensative switching
    • Compensative switching [2] does not compensate for all input codes
    • Split digital input into sum of two digital codes
    • The conversion errors reduced using compensative switching for the two new digital inputs
    • Final output is the sum of the two conversions
  
-----------------------------------------

• Needs two sets of 2-C DACs
• Needs analog summation
• Needs sophisticated algorithm for splitting the input word

Mismatch Compensation (4)

- Switching techniques
  - Alternately complementary switching
    - Roles of $C_1$ and $C_2$ are swapped alternately in the first cycle and adopt complementary switching [3] for the second conversion cycle
    - Output of the two conversions are summed (or averaged)
    - INL improved due to cancellation of major second-order error
  - Hybrid switching
    - Averaging conversion results of complementary switching and alternately complementary switching
    - Smaller INL; fourfold conversion cycles

Mismatch Compensation (5)

- Mismatch shaping
  - Using oversampling ΔΣ Modulator
    - Digital state machine to control switching sequence of a symmetric two-capacitor DAC
    - Improved linearity; better shaping for higher OSR
    - Needs 2N clock cycles for N-bit D/A


Simulated (FFT) performance of the DAC without (a) and with (b) mismatch shaping using a second-order loop filter
Mismatch Compensation (6)

- Radix-Based Digital Correction
  - Compensation in digital domain
    - Effectively a radix-$(C_1/C_2)$ conversion
      \[ V_{out} = V_{ref} \left( C_1/C_2 \right) \sum_{i=1}^{N} b_i (1 + C_1/C_2)^{-i} \]
    - Assumes known mismatch $2(C_1-C_2)/(C_1+C_2)$, or $C_1/C_2$
    - ADC-like algorithm predistorts digital input
    - Feeds predistorted digital words into the 2-C DAC
    - Better performance when DAC resolution is high
    - Needs value of mismatch, with high accuracy.
  - J. Cao et al., ISCAS 2010

Radix-based digital pre-distortion algorithm flowchart

DAC output spectra plots for (a) uncompensated condition, (b) alternately complementary switching, (c) radix-based algorithm and (d) radix-based algorithm with one extra bit.
Two-Capacitor DAC Variations

- **Time interleaved 2-C DAC**
  - Time interleaving 2-C blocks improves throughput speed
  - Capacitor mismatch *between* channels is tolerable
  - Direct-charge-transfer buffer reduces power consumption

- **Pipelined quasi-passive cyclic DAC**
  - Same operation as 2-C DAC
  - Information passed on to the last capacitor and DCT output buffer

Quasi-Passive SC Pipeline DAC

- Serial digital input, Nyquist-rate output;
- Tolerant to switch nonidealities; little glitching
- Capacitor mismatches, DCT buffer errors limit operation to 11 – 12 bit accuracy.
SC Pipeline DAC

Operation:

- Pipelined version of the two-C DAC.
- Bits are entered serially, starting with LSB controlling the charging of $C_1$.
- Charges are shared between adjacent capacitors, rippling down the pipeline.
- After delivering charge, each C is free to receive new one.
- Three clock phases needed.
- Last C voltage is buffered and read out.
Segmented SC Pipeline DAC

• For high accuracy, the pipeline DAC may be combined with a unary MSB DAC, and use dynamic element matching (DEM).
• Unary DAC with DCT buffer:
Quasi-Passive Pipeline DAC Schematic

- Operates from LSB toward MSB
- Pipelined operation by 3-bit segments of each input digital word
- Charges are shared by adjacent capacitors
- For $N$-bit conversion, it requires $N+1$ equal valued capacitors

Segmented DAC Realization

- Example of 6-bit DAC with 4+2 segmentation.

- For $N$ bits, it requires $(n_{LSB}+1)+(2^{n_{MSB}}-1)$ equal valued capacitors, where $N = n_{LSB} + n_{MSB}$. 
Multi-Segmented DAC Realization

- Example of 6-bit DAC with 2+2+2 segmentation
- For $N$ bits, it requires $(n_{LSB} + 1)C + (2^{n_{intermediate} - 1})C + (2^{n_{MSB} - 1})(2^{n_{intermediate}} C)$
  where $N = n_{LSB} + n_{intermediate} + n_{MSB}$

Fig. 6-bit DAC realization
Dynamic Element Matching (DEM)

- Multi-Segmented Quasi-Passive Pipeline DAC (7+4+4). 0.1% error.
- Response on the left is without DWA, and on the right is with DWA.

Fig. DWA Effect
ΔΣ DAC Structure

Block diagram of a ΔΣ DAC.

Single-bit DAC can be linear. For a few bits (2~4), DEM can be used.

Signal and noise spectra in a ΔΣ DAC.
ΔΣ DAC Examples

Combined DAC, DCT and filter for a multi-bit ΔΣ DAC [8].

Another ΔΣ DAC with merged DAC, DCT and SCF filter functions [15].
Micro-Power Delta-Sigma DACs

- Digital interpolation filter followed by digital D-S loop, and DCT stage performing D/A conversion and pre-filtering.
- Low-resolution SC DAC can be simple, low power.
- Easy trade-off between speed, accuracy and power dissipation.
- Passive R-C reconstruction filter may be possible.

![Diagram of DAC system with blocks for interpolation filter, ΔΣ loop, SC DAC, and filter leading to output voltage.](image)
Classification of ADCs

- “Nyquist-rate” ADCs: sample-by-sample memoryless conversion;

- “Oversampled” ADCs: output word depends on all earlier input values. Memory-assisted conversion [2].

- Generally, Nyquist-rate converters designed in the time domain, oversampled ones in the frequency domain.
Classification of Nyquist-rate ADCs

\((T=\text{clock period}, \, N=\text{resolution in bits})\)

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<tr>
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<tbody>
<tr>
<td>Parallel (flash)</td>
<td>(T)</td>
<td>(T)</td>
<td>5-9 bits</td>
<td>R string, comparators</td>
</tr>
<tr>
<td>Pipeline</td>
<td>(T)</td>
<td>(NT)</td>
<td>10-14 bits</td>
<td>SC stages+ T/H+ opamps.</td>
</tr>
<tr>
<td>Subranging (half-flash)</td>
<td>(2T)</td>
<td>(2T)</td>
<td>8-12 bits</td>
<td>R strings, comparators</td>
</tr>
<tr>
<td>Serial (Succ.appr)</td>
<td>(NT)</td>
<td>(NT)</td>
<td>7-12 bits</td>
<td>SC charge redistribution</td>
</tr>
<tr>
<td>Counting</td>
<td>(2^{NT})</td>
<td>(2^{NT})</td>
<td>16-24 bits</td>
<td>SC or CT integrator</td>
</tr>
</tbody>
</table>

Successive-Approximation-Register ADC

- Serial operation: $N$ cycles for $N$-bit resolution;
- DAC errors limit the accuracy;
- Needs S/H.
- For low speeds, the active blocks dissipate most power.
SAR ADCs [7],[8]

- The conventional SAR ADC (3 bits)

\[ E_{\text{total}} = 49 \frac{C V_{\text{ref}}^2}{8} \]

- The junction-splitting SAR ADC

\[ E_{\text{total}} = 7 \frac{C V_{\text{ref}}^2}{8} \]
Energy Loss in SAR C Arrays

Energy loss considerations (for 3 bits):

• Energy required to charge an uncharged capacitor C to voltage V is \( E = C.V^2 \). Half is lost in the switch.

• In SAR ADC, for \( V_{in} = 0 \), the initial step draws an energy \( 2C.V_{ref}^2 \) Joules, subsequent steps draw comparable amounts from \( V_{ref} \).

• In the modified array, the first step draws \( (C/2).V_{ref}^2 \), the following ones less. The total energy is less than \( C.V_{ref}^2 \). Mismatch effects may be worse.
Simpler SAR ADC Circuit

- Conventional implementation needs $2^N$ unit capacitors. Reduced cap implementation (W.Yu et al., ISCAS 2010):

Needs $2N$ clock periods for every output word.
Simpler SAR ADC

• Four capacitors and a charge copier can generate all voltages for the SAR ADC.

• In each period, an upper limit, a lower limit and their average value are developed.

• The active block acts as a charge copier during $\Phi_1 = 1$, and as a comparator during $\Phi_2 = 1$.

• Active block needs more power than in other SAR ADCs.
Faster SAR ADC Circuit [9]

- Faster implementation.
- Large spread of Cs and/or Vs.
Faster SAR ADC

- Input capacitor is charged to $V_{in}$, and then the other capacitors add or subtract charges scaled from $C.V_r$ as controlled by the comparator output bits.

- The voltages are divided by 2 in each step.

- Also possible to use scaled capacitors and unscaled voltages, or scale both $C$ and $V$.

- Concept shown only.
Junction-Splitting SAR [8]

- Shown a 3-bit junction-splitting SAR ADC.
- $V_{out}$ is determined by the ratio of the capacitances, not by the absolute values.
- All blocks are appended to the capacitor array one-by-one, to generate the desired output voltage.
- Total capacitance: $2^N \cdot C$, where C is the unit capacitance.
- The power consumption for $V_{in}=0$ is

$$V_{ref}^2 \cdot C \cdot \left(1 - \frac{1}{2^N}\right)$$

Saves 75% average power compared to a conventional SAR ADC.

Pipeline SAR ADC

- Provides an output word each clock period – faster.
- Uses passive SC S/Hs and tapered DACs – low power.

Parasitic Capacitance Effects

If $C_s = C_{dac,tot} = C$, then

$$V_1' - V_{dac}' = (V_1 - V_{dac}) \cdot \frac{C}{C + C_P}$$
Sampling Capacitor Splitting

- Circuit diagram showing the connection of capacitors and switches labeled from C11 to C17, S1 to S2, S7, and S1a, S2a, S7a.

- The diagram illustrates the sampling process using capacitors and switches arranged in series and parallel configurations.

- The purpose of the diagram is likely to explain the principles of capacitor splitting in a sampling circuit.

- Further details or explanations may be necessary to fully understand the operation and functionality depicted in the diagram.
Parasitic-Insensitive Sampling

- For differential architecture.

- Insensitive to the input parasitic caps of the comparators.

- Insensitive to the parasitic caps in the sampling paths.
Simulation Results

- All switches in the sampling parts are real. Sampling frequency is 1GHz.

SNR = 39.8 dB

Magnitude (dBFS)

Frequency (fs)
Junction-Splitting in Pipelined SAR ADC

For 8-bit SAR ADC:

Conventional
256 C, 1X speed, 1X power consumption

Junction splitting
256 C, 1X speed, 0.25X power consumption

Junction-Splitting pipeline
512 C, 8X speed, 2X power consumption

* J. Lin, W. Yu and G. C. Temes, “Micro-power time-interleaved and pipelined SAR ADCs,” ISCAS 2010
Two-Step Split-Junction SAR ADC

For a 6-bit SAR

- First 3 bits (MSB) coarse quantization, the same as split-junction SAR
- Last 3 bits (LSB) fine quantization, interpolate with DAC1 and DAC2

Save 8X capacitor area and power consumption.

Power Consumption vs. Output Digital Code

![Graph showing power consumption vs. output digital code for different ADC types: Conventional SAR ADC, Conventional Pipelined SAR ADC, Junction-Splitting/Segmented Pipelined SAR ADC, and Hybrid SAR ADC. The graph plots normalized switching energy against output digital code.]
## Comparison of Different SAR ADCs

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Throughput (word/period)</th>
<th>(P_{\text{Dynamic}}/CV_{\text{ref}}^2) for code 00…0</th>
<th>Total Capacitance</th>
<th>Number of Switches</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conv. Single SAR ADC</td>
<td>1/N</td>
<td>( \frac{5}{6} \cdot 2^N - \frac{1}{2} \cdot 2^{-N} - 1 )</td>
<td>(2^N \cdot C)</td>
<td>(2 \cdot (N + 1))</td>
</tr>
<tr>
<td>Energy-efficient Single SAR ADC</td>
<td>1/N</td>
<td>(1 - 2^{-N})</td>
<td>(2^N \cdot C)</td>
<td>(3 \cdot N - 1)</td>
</tr>
<tr>
<td>Conv. T.I. SAR ADC</td>
<td>1</td>
<td>(\frac{5}{6} \cdot 2^N - \frac{1}{2} \cdot 2^{-N} - 1)</td>
<td>(N \cdot 2^N \cdot C)</td>
<td>(2 \cdot N \cdot (N + 1))</td>
</tr>
<tr>
<td>T.I. Segmented SAR ADC</td>
<td>1</td>
<td>(1 - 2^{-N})</td>
<td>((2^{N+1} - 2) \cdot C)</td>
<td>(\frac{1}{3} N^3 + N^2 + \frac{2}{3} N)</td>
</tr>
<tr>
<td>Conv. Pipelined SAR ADC</td>
<td>1</td>
<td>(N - 1 + 2^{-N})</td>
<td>((2^{N+1} - 2) \cdot C)</td>
<td>(\frac{1}{2} N^2 + \frac{1}{2} N - 1)</td>
</tr>
<tr>
<td>Segmented Pipelined SAR ADC</td>
<td>1</td>
<td>(1 - 2^{-N})</td>
<td>((2^{N+1} - 2) \cdot C)</td>
<td>(\frac{1}{3} N^3 + 2N^2 + \frac{2}{3} N)</td>
</tr>
<tr>
<td>Two-step (hybrid) SAR ADC</td>
<td>(1/(N+1))</td>
<td>(1 - 2^{-\frac{N}{2}}) \text{ N is an even.} (\frac{N}{2}^{\frac{N+1}{2}} \cdot C) \text{ N is an even.}</td>
<td>(\frac{1}{4} N^2 + \frac{7}{2} N + 1) \text{ N is an even.}</td>
<td>(\frac{1}{4} N^2 + 4N + \frac{19}{4}) \text{ N is odd.}</td>
</tr>
</tbody>
</table>
ADC Architectures

Delta-Sigma (\(\Delta\Sigma\)) Modulators

\[ U(z) \xrightarrow{1-z^{-1}} \frac{z^{-1}}{1-z^{-1}} \xrightarrow{\text{DAC}} V(z) \]

\[ U(z) \xrightarrow{1-z^{-1}} \frac{z^{-1}}{1-z^{-1}} \xrightarrow{\text{ADC}} E(z) \]

\[ STF(z) = z^{-1} \]
\[ NTF(z) = 1 - z^{-1} \]

Incremental ADCs: $\Delta \Sigma$ ADCs which are reset after each conversion. Properties:

- Flexible trade-off between OSR and power dissipation;
- Limited memory – stable and not tonal;
- Well suited for instrumentation and measurement (I&M) applications;
- High absolute accuracy possible;
- Allows for accurate gain and offset error correction;
- Easily multiplexed, or operated intermittently.
- Decimation filter simpler, easily optimized for SNR.
Incremental ADC - Publications

• First incremental ADC (bipolar, 17-bit resolution, first-order $\Delta\Sigma$ loop)

• Further research (CMOS, 16-bit resolution, first-order $\Delta\Sigma$ loop)

• Multi-Stage Noise Shaping (MASH) incremental ADC (two first-order $\Delta\Sigma$ loops)

• 22-bit incremental ADC (third-order $\Delta\Sigma$ loops, 0.3 mW power consumption)

• Wideband applications (low OSR, 7th-order MASH)
Incremental ADC – Commercial ADCs

Sometimes referred to as *charge-balancing* $\Delta\Sigma$ ADCs, *one-shot* $\Delta\Sigma$ ADCs or *no-latency* $\Delta\Sigma$ ADCs.

- **AD77xx product family, Analog Devices**
  16-bit ~ 24-bit resolution, 1~10 channels, 60~2.5M SPS

- **ADS124x product family, Burr-Brown (Texas Instruments)**
  24-bit resolution, 4~8 channels, 15 SPS

- **CS55xx product family, Cirrus Logic**
  24-bit resolution, 6.25~3840 SPS

- **LTC24xx product family, Linear Technology**
  16-bit ~ 24-bit resolution, 1~16 channels, 6.9~8000 SPS
Low-Distortion Third-Order Structure (1)

\[
U(z) \overset{D}{\rightarrow} \frac{z^{-1}}{1 - z^{-1}} \overset{c_1}{\rightarrow} \frac{z^{-1}}{1 - z^{-1}} \overset{c_2}{\rightarrow} \frac{z^{-1}}{1 - z^{-1}} \overset{a_2}{\rightarrow} v_3[k] \overset{Q}{\rightarrow} Y(z) \overset{d_{out}[k]}{\rightarrow}
\]

\[
|v_3(k)| \leq V_{ref}
\]

\[
Y(z) = U(z) + (1 - z^{-1})^L Q(z)
\]

\[
U(z) - Y(z) = -(1 - z^{-1})^L Q(z)
\]

Only quantization noise \( Q(z) \) propagates through the integrators.

Low-Distortion Third-Order Structure (2)

\[
u - \frac{3 \cdot 2}{M(M-1)(M-2)} \sum_{m=0}^{M-1} \sum_{l=0}^{m-1} \sum_{k=0}^{l-1} d_{out}[k]V_{ref} \leq \frac{3 \cdot 2 \cdot V_{ref}}{b c_1 c_2 M(M-1)(M-2)}
\]

\[
D = \frac{3 \cdot 2}{M(M-1)(M-2)} \sum_{m=0}^{M-1} \sum_{l=0}^{m-1} \sum_{k=0}^{l-1} d_{out}[k]V_{ref}
\]

\[
|\varepsilon| = |u - D| \leq \frac{3 \cdot 2 \cdot V_{ref}}{b c_1 c_2 M(M-1)(M-2)}
\]

Offset Correction in Integrators (1)

Fractal sequencing: a generalization of chopper stabilization. For a cascade of integrators, chopping is inadequate: the integrator outputs for 1 mV offset are 1,-1,1,-1 -> 1,0,1,0 -> 1,1,2,2, etc.

Change the first opamp input/output polarity according to fractal sequencing

\[ S_1 = (+ -) \]
\[ S_2 = (S_1 \bar{S}_1) = ((+ -)(- +)) \]
\[ \ldots \]
\[ S_n = (S_{n-1} \bar{S}_{n-1}) \]

If \( S_n \) is used for an \( n \)-th order modulator, and the modulator runs for \( M \) clock periods (where \( M/2^n \) is an integer) the first opamp offset will be cancelled.

Multiplexed Incremental ADC

ADC may be shared between $N$ channels. An FIR decimation filter need not be reset. A low-distortion modulator with FIR NTF needs no reset either.
Optimization of Incremental ADC

\[ v(n) = \left[ stf'(k) * u(k) + stf'(k) * t(k) + ntf'(k) * q(k) \right]_{M,n} \]

\( v(n) \) is the single output value obtained in the \( n \)th conversion cycle.
\( u(k) \) is the input signal.
\( t(k) \) is the input-referred thermal noise.
\( q(k) \) is the quantization noise.
\( stf'(k) \) is the impulse response of the overall signal transfer function \( STF(z)H(z) \).
\( ntf'(k) \) is the impulse response of the overall noise transfer function \( NTF(z)H(z) \).
\( H(z) \) is the transfer function of the decimation filter.

Both \( stf'(k) \) and \( ntf'(k) \) have finite lengths (length=\( M \)), where \( M \) is the number of clock periods in each conversion cycle.

Noise Optimization in Incremental ADC

To minimize the overall output noise power, find $h$ from

$$\min_h v_n^2 = h^T \cdot O \cdot h,$$

where

$$O = \frac{5kT}{C_{in}} S^T S + \frac{\Delta^2}{6} N^T N$$

$S$ and $N$ are matrices constructed from the $stf(k)$ and $ntf(k)$ sequences.

The problem can be formulated as quadratic programming, or solved analytically for the optimum $h(n)$ using Lagrange multiplier method.

The digital filter is FIR; it can be realized simply as a single multiply-accumulate block.

## Micro-power ADC for Biopotential Sensor

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>IBM 90nm</td>
</tr>
<tr>
<td>VDD</td>
<td>1.2 V</td>
</tr>
<tr>
<td>Operating Clock</td>
<td>1MHz</td>
</tr>
<tr>
<td>Signal Bandwidth</td>
<td>1kHz</td>
</tr>
<tr>
<td>No. of multiplexed input channels</td>
<td>2</td>
</tr>
<tr>
<td>Nyquist-Rate Data Conversion Rate</td>
<td>2 ksample/sec</td>
</tr>
<tr>
<td>Oversampling Ratio</td>
<td>256</td>
</tr>
<tr>
<td>0dB full-scale voltage</td>
<td>1.2V single-ended</td>
</tr>
<tr>
<td>Max. Input Signal</td>
<td>0.5V(_{pp}) single-ended</td>
</tr>
<tr>
<td></td>
<td>1.0V(_{pp}), fully-differential</td>
</tr>
<tr>
<td>SNDR</td>
<td>&gt;74 dB</td>
</tr>
<tr>
<td>Resolution</td>
<td>&gt;12 bit</td>
</tr>
<tr>
<td>Power</td>
<td>87.65 (\mu)W</td>
</tr>
</tbody>
</table>

FoM = \( \frac{\text{Power}}{2^{\text{bit}} \cdot 2 \cdot \text{BW}} \) = 1.69 \(pJ/\text{Conv.}\)
Block Diagram of the Incremental ADC

Vin

\( \frac{Z^{-1}}{1-Z^{-1}} \)

Adder

Digital Filter

Dout

Integrator

Adder

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Low-Power Opamp Circuit

Total static current is 1.3 uA.
Auto-Zeroing Comparator

- Static current for each preamp is 50 nA.
- Latches draw no static current.
Simulated PSD of $\Delta\Sigma$ Modulator

- **Conditions**
  - IBM 90nm Technology
  - Sampling clock: 1.024MHz
  - OSR: 256
  - Signal frequency: 375 Hz
  - Single-ended amplitude: $V_{pp}=0.5V$
  - Fully-differential amplifier: $V_{pp}=1.0V$

- SNDR = 85.1 dB

- ADC in incremental mode is being simulated now.

- Simulated FoM

\[
\frac{\text{Power}}{2^{\text{bit}} \cdot 2 \cdot \text{BW}} = \frac{87.65\mu W}{2^{14} \cdot 2 \cdot 2kHz} = 1.69\text{pJ/conv.}
\]
MUXed Incremental ADC Design (W. Yu)

Specifications
- Multiple channels ($N = 20$)
- Narrow bandwidth ($f_B = 3$ kHz)
- SNDR (100 dB)

Design Procedure
- Maximum conversion time for one channel: $T_w = 1/(2Nf_B) = 8.33$ µs
- Maximum number of samples in one conversion cycle: $M_{\text{max}} = T_wf_c = 250$
- Modulator design: $NTF = \frac{(z - 1)^3}{(z - 0.5701)(z^2 - 1.39z + 0.6149)}$
System Design (Cont.)

- Noise budget: 90% thermal noise and 10% quantization noise
- Total noise allowed: $P_{tot} = 10^{-10} V^2$ (100 dB SNR for 1 V$^2$ output power)
- Estimation of the minimum $MC_{in}$
  
  $P_t \leq 0.9 P_{tot}$  $MC_{in} \geq 460$ pF
- Choose $M = 230$ and $C_{in} = 2$ pF
- Decimation filter optimization

Matlab Simulation

Conversion error versus DC input voltage

-140
-120
-100
-80
-60
-40
-20
DC input voltage (V)
Conversion error (dBFS)
Simulation (quantization noise only)
Theoretical (thermal)
Theoretical (quantization)
Matlab Simulation

SQNR versus input amplitude for 507 Hz sine-wave input

Peak SQNR = 114 dB
DR = 111 dB
Die Micrograph

INT1
DWA Buffer

INT2
INT3
Adder

Decoupling Caps
Measurement Results

The spectrum of the modulator output when the modulator is running as a single sampling ΔΣ modulator for a −2.5 dBFS sine wave input.

ΔΣ modulator mode
SNR = 86.8 dB
SNDR = 83.0 dB
OSR = 230
$f_s = 10 \, \text{MHz}$

Power consumption:
6.6 mW (total)
3.8 mW (analog)
2.8 mW (digital)
Measurement Results (Cont.)

Incremental mode
optimal decimation filter
SNR = 83.7 dB
SNDR = 81.5 dB
cascaded integrator filter
SNR = 82.3 dB
SNDR = 79.7 dB
OSR = 230
$f_s = 10\, \text{MHz}$

*Power consumption:*
6.6 mW (total)
3.8 mW (analog)
2.8 mW (digital)

The spectrum of the incremental ADC output (after decimation) with optimal decimation filter (blue line) and with traditional cascaded integrator decimation filter (red line) for a $-3.4\, \text{dBFS}$ sine wave input.
Measurement Results (Cont.)

ΔΣ modulator mode:  

before digital correction  
SNR = 80.1 dB  
SNDR = 73.4 dB  

after digital correction  
SNR = 71.3 dB  
SNDR = 63.6 dB  

OSR = 230  
f_s = 10 MHz  

Power consumption:  
6.6 mW (total)  
3.8 mW (analog)  
2.8 mW (digital)  

The spectrum of the modulator output (continuously-running single sampling ΔΣ modulator) before (red line) and after digital compensation (blue line). The DWA was turned off.
Advantages of extended-range ADC:

1. Incremental ΔΣ modulator operates at oversampled frequency $f_s$.
2. Feedforward topology is used to lower the signal swings.
3. The 2$^{nd}$ stage ADC converts the residual error at the 1$^{st}$ stage output.
4. The 2$^{nd}$ stage may use a SAR ADC, with an operating frequency $f_s/M$. 

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Operation of Extended-Counting ADC

- After $M$ cycles, $v_2(M)$ becomes

$$v_2(M) = a_1 \cdot a_2 \cdot \frac{M(M-1)}{2} \cdot v_{in} + a_1 \cdot a_2 \cdot V_{ref} \cdot \sum_{j=1}^{M} (M-j) \cdot Y(j)$$

- $v_2(M)$ is converted by the 2$^{nd}$ ADC and combined with the triangularly-weighted output sequence.

- The overall quantization error is ideally only the quantization error of the SAR ADC:

$$E_{Q-ADC} = \frac{2}{a_1 \cdot a_2 \cdot M \cdot (M-1)} \cdot E_{Q-SAR}$$
Circuit Implementation [1]

SAR ADC
- 11-bit resolution
- Dual-capacitor array to reduce the total input capacitance to 3 pF, using a unit cap 48 fF
- Conversion in 11 cycles of charge redistribution.

Incremental ΔΣ Modulator
- Clock frequency = 45.2 MHz.
- OSR = 45.
Measured Results

- Signal: -6dB, 110kHz
- peak SNDR is 86.3 dB, SFDR is 97 dB
- ADC achieved 90.1dB dynamic range.
- 38 mW power dissipation (excluding output drivers), out of which 23 mW is consumed in the 1st opamp, 9 mW in the 2nd opamp, 1 mW in the SAR, less than 5 mW in all digital blocks.
References on DACs

References


References on ADCs


[12] S.-W. Chen and R. Brodersen, “A 6b 600MS/s 5.3mW asynchronous ADC in 0.12um CMOS”
References on Extended Counting ADCs

