Name: ________________________________

CS/ECE472 Midterm #2
SPRING 2011

NAME: ________________________________
Student ID#: __________________________

OPEN BOOK, OPEN NOTES. You can use material from previous exams, the book, etc. You CANNOT use other people for help.

SHOW YOUR WORK. ANSWERS ONLY will be treated as if cheating may have occurred, ESPECIALLY SINCE THIS IS A TAKEHOME EXAM.

OUT: May 23, 2011
IN: Jun 01, 2011

Your signature is your promise that you have not cheated and will not cheat on this exam, nor will you help others to cheat on this exam. NOTE: If exam is not signed, it will not be scored.

Signature: ________________________________

ABET Requirements:
1. Use various metrics to calculate the performance of a computer system
2. Identify the addressing mode of instructions
3. Determine which hardware blocks and control lines are used for specific instructions
4. Demonstrate how to add and multiply integers and floating-point numbers using twos complement and IEEE floating point representation
5. Analyze clock periods, performance, and instruction throughput of single-cycle, multi-cycle, and pipelined implementations of a simple instruction set
6. Detect pipeline hazards and identify possible solutions to those hazards
7. Show how cache design parameters affect cache hit rate
8. Map a virtual address into a physical address

Question 1 _________ (20 points) (ABET #2, #3)
Question 2 _________ (15 points) (ABET #6)
Question 3 _________ (15 points) (ABET #5, #1)
Question 4 _________ (10 points) (ABET #5, 7)
Question 5 _________ (10 points) (ABET #8)
Question 6 _________ (15 points) (ABET #1)
Question 7 _________ (15 points) (power; parallelism)

TOTAL ___________
1. (20 points) Consider the following instruction through the implementation on page 6 of this test.

<table>
<thead>
<tr>
<th>Address of instr.</th>
<th>Instruction</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x1FF0 F000</td>
<td>beq $t7, $t3, -31</td>
</tr>
</tbody>
</table>

After the instruction is decoded:
What are Instruction bits 25-21: 0 1 1 1 1
What are Instruction bits 20-16: 0 1 0 1 1
What is ALUSrc: O (0, 1, or X <- don't care)
What is MemtoReg: X (0, 1, or X <- don't care)
What is RegDst: X (0, 1, or X <- don't care)
What is Branch: 1 (0, 1, or X <- don't care)

Consider the following instruction through the implementation on page 7 of this test.

<table>
<thead>
<tr>
<th>Address of instr.</th>
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</tr>
</thead>
<tbody>
<tr>
<td>0x1FF0 F000</td>
<td>beq $t7, $t3, -31</td>
</tr>
</tbody>
</table>

What is ALUSrcA during cycle 1: O (0, 1, or X <- don't care)
What is ALUSrcA during cycle 2: X (0, 1, or X <- don't care)
What is ALUSrcA during cycle 3: 1 (0, 1, or X <- don't care)

Assuming the branch is taken, what address is loaded into the PC? 0x1FFF 0F88

2. (15 points) Assume that you have a pipelined implementation of MIPS with a perfect cache. Draw the pipelining diagram for the code along the left side. I have started the diagram for you with the first statement. **Indicate all data dependencies by circling the registers in the code.** Indicate all necessary forwarding from the output of one functional unit to the input of another functional unit. Indicate all necessary stalls with a nop. Keep everything that happens in the same clock cycle in a straight column. You do not have to shade the active units. Assume BRANCH NOT TAKEN

```
lw $2, 64($4)
lw $3, 0($2)
beq $2, $3, NEXT
lw $5, 4($3)
```
3. (15 points) The CPI of a machine with a perfect cache is 1.8 for a certain benchmark.

Now, assume a L1 instruction cache miss rate of 4.5% and a L1 data cache miss rate of 17%.
Assume the miss penalty (for either L1 caches) is 8 cycles. The hit time is 1.5 cycle (L1 cache).
Assume a L2 instruction cache miss rate of 3% and a L2 data cache miss rate of 7%.
Assume the miss penalty (for either L2 caches) is 900 cycles. The hit time is 40 cycles (L2 cache).

The frequency of data access instructions in this benchmark is 11%.

How much faster is the machine with the perfect cache than the one with the imperfect L1 and L2 caches? Otherwise the machines are identical and running the same code. Express your answer either as a fraction or as a decimal rounded to the hundredths place. (XX.XX) Your answer should be > 1.

SHOW ALL WORK.

4. (10 points) Assume we have a 32 KB cache, 16-way set associative cache. (KB = 2^10 bytes)
The block size is 16 words.
Given a 32-bit physical address, divide up all the bits and indicate what they are used for to find and access the requested word in the cache. Do NOT draw the cache entries, the mux, the AND gate, ... Just indicate exactly how many bits and which bits of the address are used for each purpose. Label your groups of bits with their purpose.
5. (10 points) Assume a 48-bit virtual address and a 16-bit physical address. The page size is 1 KB. How many entries are there in the page table? Express your answer in powers of 2. Show your work for this problem. (KB = 2^10 bytes)

\[ 2^{38} \]

6. (15 points) A) Write a loop in MIPS that first multiplies each int in an array size of 8 by the constant ‘16’ using only shifts (not multiplies), and then adds it to a running sum. Use my registers ($t0, $t1, $t2) as declared in the comments. Use only MIPS core instructions (and a new instruction ‘mult’). Feel free to use registers $t1 - $t7.

```
# $t0 holds the address of the first int in the array
add $t1, $t0, 32
add $t2, $zero, 0

LP:       UNROLLED:
add $t1, $t1, $t1
lw $t3, 0($t1)
sl $t4, $t3, 4,
add $t2, $t4, $t2-1
bne $t1, $t0, LP
```

B) Unroll your loop (just the code that starts at LP) so that it executes 1 time and has no data hazards. Write your code to the right of your code from part A).
7) (15 points) Assume you have two processors: one that operates on the normal sequential loop code in problem #6, and another that operates on the loop-unrolled version of problem #6, and can execute on four parallel instructions simultaneously.

PROCESSOR-1 (NORMAL):
VDD=1.0V  
f = 1GHz  
Capacitance (C) = 1e-9 F (for entire PROCESSOR)

PROCESSOR-2 (4-cores):
VDD=0.6V  
f = 250MHz  
Capacitance (C) = 0.4e-9 F (for each core)

PROCESSOR-2 can execute on 4 arithmetic operations simultaneously, if they are parallel. It CANNOT operate on a LW and a MULT simultaneously, but it can do a MULT and another MULT, if they are independent MULTs.

A) What is the average power consumption, of PROCESSOR-1 and PROCESSOR-2, over this entire code sequence? Assume that an idle core is burning the same power as an active core.

Solution for #7 will vary based on answer from #6.

B) What is the energy-consumed for each PROCESSOR (both 1 and 2) in executing the entire code sequence for Problem 6? Assume the energy consumed for executing one instruction is CV^2. For example, for four instructions in parallel, the energy will be 4*CV^2.

C) What is the execution time for each PROCESSOR, using both these code sequences from Problem 6?