Introduction

In this project you will work in groups of two to use what you learned about adders from project 1 to model and simulate the 16-bit ALU Design discussed in Section C.5 (on CD) of the book using both the ripple adder and carry look-ahead adder. Your ALU will take two 16-bit operands and a 3-bit opcode and generate a 16-bit result, overflow flag, zero flag and carry-out bit.

1. Figure 2 shows the schematic of the ALU Slice discussed in Section C.5 of the book (CD). Write a new Verilog module that describes this using the fulladder module discussed earlier and a new mux4 module that implements a 4:1 mux. Call this module ALU_slice. Simulate it to make sure that it operates correctly.

Note that Binvert will be derived from the MSB of your opcode and that for a subtract operation you will invert the B operand and then add one, i.e. carry-in_0 = 1 (two’s complement).

2. The SLT (Set on less than) operation returns a value of 1 (hex 0001) as the result if A<B. Consider what input cases for ADD, SUB and SLT operations will result in an overflow (or underflow) condition. Create another Verilog module that extends the ALU_slice module to perform the additional tasks necessary for the most significant bit of the ALU (i.e., generating “Set”, and “Overflow”). Call this module ALU_slice_MSB. Simulate it to make sure that it operates correctly.

3. Create a top-level module called ALU16 which contains instances of the ALU_slice and ALU_slice_MSB modules connected to form a 16-bit ALU. Include hardware to generate the “Zero” output. Simulate it to make sure that it operates correctly.
4. Modify your design to use CLA addition instead of ripple adder addition.

5. **Hand in code listings for your Verilog modules** for the basic ALU and carry look-ahead ALU **along with simulation waveforms** (screenshots are great) which show each of the ALU operations functioning correctly for a variety of different inputs. Be sure to check overflow and underflow conditions. **Add labels to your simulation diagrams to explain what operations are being performed in each test case and in different parts of the waveform.**

**Turn in ONE pdf document with all the necessary images and descriptions.**