ECE 627 PROJECT

Design of a Delta-Sigma A/D Converter

Due: June 11, 2013, 5 pm.

Design a delta-sigma ADC for the following specifications:

<table>
<thead>
<tr>
<th>Specification</th>
<th>Requirement</th>
</tr>
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<tbody>
<tr>
<td>Signal bandwidth</td>
<td>0 – 10 kHz</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>Less than 6 MHz</td>
</tr>
<tr>
<td>Accuracy</td>
<td>At least 20 bits</td>
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</tbody>
</table>

Design tasks:

1. Choose an architecture. Justify your choice in terms of performance, power dissipation, complexity, etc.
2. Carry out the theoretical design: find the STF and NTF, draw the block diagram in terms of delay elements, adders, comparators, DACs, etc.
3. Plot the NTF and STF gain-frequency curves and the pole-zero patterns.
4. Compute and plot the SNR vs. input sine-wave amplitude characteristics.
5. Perform scaling of the coefficients for optimum dynamic range performance.
6. Design and draw the switched capacitor realization of the ADC loop, considering the $kT/C$ noise.
7. Simulate the switched capacitor circuit using SWITCAP or any other CAD tool.
8. Find the minimum slew rate needed by the opamps if the output is allowed to slew only for 20% of the total settling time.
9. Design and draw the block diagram of a decimation filter to follow the loop.
10. Simulate the overall performance of the complete ADC in MATLAB.
11. Analyze and describe the nonideal effects influencing the performance: finite opamp gain, finite opamp bandwidth, slew rate, capacitor mismatch, analog noise, digital round-off errors, etc

The report must be typed and short (5-6 pages maximum, not counting the Appendix). It should contain a Table summarizing the performance, including the total capacitance value (after optimization), an Appendix with the MATLAB code, and any netlists used for circuit simulations.