FEATURES
High Performance Member of Pin-Compatible TxDAC Product Family
125 MSPS Update Rate
12-Bit Resolution
Excellent Spurious Free Dynamic Range Performance
SFDR to Nyquist @ 5 MHz Output: 79 dBc
Differential Current Outputs: 2 mA to 20 mA
Power Dissipation: 185 mW @ 5 V
Power-Down Mode: 20 mW @ 5 V
On-Chip 1.20 V Reference
CMOS-Compatible +2.7 V to +5.5 V Digital Interface
Package: 28-Lead SOIC and TSSOP
Edge-Triggered Latches

APPLICATIONS
Wideband Communication Transmit Channel:
  Direct IF
  Base stations
  Wireless Local Loop
  Digital Radio Link
  Direct Digital Synthesis (DDS)
  Instrumentation

PRODUCT DESCRIPTION
The AD9752 is a 12-bit resolution, wideband, second generation member of the TxDAC family of high performance, low power CMOS digital-to-analog converters (DACs). The TxDAC family, which consists of pin compatible 8-, 10-, 12-, and 14-bit DACs, is specifically optimized for the transmit signal path of communication systems. All of the devices share the same interface options, small outline package and pinout, thus providing an upward or downward component selection path based on performance, resolution and cost. The AD9752 offers exceptional ac and dc performance while supporting update rates up to 125 MSPS.

The AD9752's flexible single-supply operating range of 4.5 V to 5.5 V and low power dissipation are well suited for portable and low power applications. Its power dissipation can be further reduced to a mere 65 mW, without a significant degradation in performance, by lowering the full-scale current output. Also, a power-down mode reduces the standby power dissipation to approximately 20 mW.

The AD9752 is manufactured on an advanced CMOS process. A segmented current source architecture is combined with a proprietary switching technique to reduce spurious components and enhance dynamic performance. Edge-triggered input latches and a 1.2 V temperature compensated bandgap reference have been integrated to provide a complete monolithic DAC solution. The digital inputs support +2.7 V to +5 V CMOS logic families.

*Protected by U.S. Patents 5450084, 5568145, 5689257, 5612697 and 5703519. Other patents pending.

REV. 0

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# AD9752—SPECIFICATIONS

## DC SPECIFICATIONS (T_MIN to T_MAX, AVDD = +5 V, DVDD = +5 V, I_OUTF = 20 mA, unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
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<tr>
<td>RESOLUTION</td>
<td>12</td>
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<td></td>
<td>Bits</td>
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<tr>
<td>DC ACCURACY</td>
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<tr>
<td>Integral Linearity Error (INL)</td>
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<tr>
<td>$T_A = +25^\circ C$</td>
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<td>+1.5</td>
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<td>LSB</td>
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<td>+1.0</td>
<td>LSB</td>
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<tr>
<td>ANALOG OUTPUT</td>
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<td></td>
<td></td>
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<tr>
<td>Offset Error</td>
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<td></td>
<td>+0.02</td>
<td>% of FSR</td>
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<tr>
<td>Gain Error (Without Internal Reference)</td>
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<td>±0.5</td>
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<td>% of FSR</td>
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<tr>
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<td>-5</td>
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<td>Full-Scale Output Current^4</td>
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<td>20.0</td>
<td>mA</td>
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<td>Output Resistance</td>
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<td>pF</td>
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<td></td>
<td></td>
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<td>Reference Output Current^3</td>
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<td></td>
<td>nA</td>
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<td>REFERENCE INPUT</td>
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<td>Small Signal Bandwidth</td>
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<td>MHz</td>
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<td>TEMPERATURE COEFFICIENTS</td>
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<td>Offset Drift</td>
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<td>ppm of FSR/C</td>
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<td>Gain Drift (Without Internal Reference)</td>
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<td>Reference Voltage Drift</td>
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<tr>
<td>Supply Voltages</td>
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<td>AVDD</td>
<td>4.5</td>
<td>5.0</td>
<td>5.5</td>
<td>V</td>
</tr>
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<td>DVDD</td>
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<td>5.0</td>
<td>5.5</td>
<td>V</td>
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<td>Analog Supply Current (I_AVDD)^4</td>
<td>34</td>
<td>39</td>
<td></td>
<td>mA</td>
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<tr>
<td>Digital Supply Current (I_DVDD)^5</td>
<td>3</td>
<td>5</td>
<td></td>
<td>mA</td>
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<td>Supply Current Sleep Mode (I_AVDD)^6</td>
<td>4</td>
<td>8</td>
<td></td>
<td>mA</td>
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<td>Power Dissipation^2 (5 V, I_OUTF = 20 mA)</td>
<td>185</td>
<td>220</td>
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<td>mW</td>
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<td>Power Supply Rejection Ratio^3—AVDD</td>
<td>-0.4</td>
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<td>+0.4</td>
<td>% of FSR/V</td>
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<tr>
<td>Power Supply Rejection Ratio^3—DVDD</td>
<td>-0.025</td>
<td></td>
<td>+0.025</td>
<td>% of FSR/V</td>
</tr>
</tbody>
</table>

## OPERATING RANGE

-40°C to +85°C

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**NOTES**

1. Measured at IOUTA, driving a virtual ground.
2. Nominal full-scale current, I_OUTF, is 32 x the Ialborg current.
3. Use an external buffer amplifier to drive any external load.
4. Requires +5 V supply.
5. Measured at f_CLOCK = 25 MSFPS and I_OUTF = static full scale (20 mA).
6. Logic level for SLEEP pin must be referenced to AVDD. Min V_HH = 3.5 V.
7. 1.5% Power supply variation.

Specifications subject to change without notice.
**DYNAMIC SPECIFICATIONS**

(T_MIN to T_MAX, AVDD = +5 V, DVDD = +5 V, I_OUPS = 20 mA, Differential Transformer Coupled Output, 50 Ω Doubly Terminated, unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
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<tr>
<td><strong>DYNAMIC PERFORMANCE</strong></td>
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<td></td>
<td></td>
<td></td>
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<tr>
<td>Maximum Output Update Rate (f_CLOCK)</td>
<td>125</td>
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<td></td>
<td>MSPS</td>
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<td>Output Setting Time (tSET) (to 0.1%) (^1)</td>
<td>35</td>
<td></td>
<td></td>
<td>ns</td>
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<tr>
<td>Output Propagation Delay (tPD)</td>
<td>1</td>
<td></td>
<td></td>
<td>ns</td>
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<tr>
<td>Glitch Impulse</td>
<td>5</td>
<td></td>
<td></td>
<td>pV·s</td>
</tr>
<tr>
<td>Output Rise Time (10% to 90%) (^1)</td>
<td>2.5</td>
<td></td>
<td></td>
<td>ns</td>
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<tr>
<td>Output Fall Time (10% to 90%) (^1)</td>
<td>2.5</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Output Noise (I_OUPS = 20 mA)</td>
<td>50</td>
<td></td>
<td></td>
<td>pA/√Hz</td>
</tr>
<tr>
<td>Output Noise (I_OUPS = 2 mA)</td>
<td>30</td>
<td></td>
<td></td>
<td>pA/√Hz</td>
</tr>
</tbody>
</table>

**AC LINEARITY**

Spurious-Free Dynamic Range to Nyquist

\[ f_{CLOCK} = 25 \text{ MSPS}; f_{OUT} = 1.00 \text{ MHz} \]

0 dBFS Output

\[ T_A = +25^\circ C \]

-6 dBFS Output

\[ f_{CLOCK} = 50 \text{ MSPS}; f_{OUT} = 1.00 \text{ MHz} \]

-12 dBFS Output

\[ f_{CLOCK} = 50 \text{ MSPS}; f_{OUT} = 2.51 \text{ MHz} \]

\[ f_{CLOCK} = 50 \text{ MSPS}; f_{OUT} = 5.02 \text{ MHz} \]

\[ f_{CLOCK} = 50 \text{ MSPS}; f_{OUT} = 14.02 \text{ MHz} \]

\[ f_{CLOCK} = 50 \text{ MSPS}; f_{OUT} = 20.2 \text{ MHz} \]

\[ f_{CLOCK} = 100 \text{ MSPS}; f_{OUT} = 2.5 \text{ MHz} \]

\[ f_{CLOCK} = 100 \text{ MSPS}; f_{OUT} = 5 \text{ MHz} \]

\[ f_{CLOCK} = 100 \text{ MSPS}; f_{OUT} = 20 \text{ MHz} \]

\[ f_{CLOCK} = 100 \text{ MSPS}; f_{OUT} = 40 \text{ MHz} \]

Spurious-Free Dynamic Range within a Window

\[ f_{CLOCK} = 25 \text{ MSPS}; f_{OUT} = 1.00 \text{ MHz} \]

84 | 93 | dBc |

\[ f_{CLOCK} = 50 \text{ MSPS}; f_{OUT} = 5.02 \text{ MHz}; 2 \text{ MHz Span} \]

86 | dBc |

\[ f_{CLOCK} = 100 \text{ MSPS}; f_{OUT} = 5.04 \text{ MHz}; 4 \text{ MHz Span} \]

86 | dBc |

Total Harmonic Distortion

\[ f_{CLOCK} = 25 \text{ MSPS}; f_{OUT} = 1.00 \text{ MHz} \]

\[ T_A = +25^\circ C \]

-82 | -74 | dBc |

\[ f_{CLOCK} = 50 \text{ MHz}; f_{OUT} = 2.00 \text{ MHz} \]

-76 | dBc |

\[ f_{CLOCK} = 100 \text{ MHz}; f_{OUT} = 2.00 \text{ MHz} \]

-76 | dBc |

Multitone Power Ratio (8 Tones at 110 kHz Spacing)

\[ f_{CLOCK} = 20 \text{ MSPS}; f_{OUT} = 2.00 \text{ MHz to 2.99 MHz} \]

0 dBFS Output

81 | dBc |

-6 dBFS Output

81 | dBc |

-12 dBFS Output

85 | dBc |

-18 dBFS Output

86 | dBc |

NOTES

\(^1\) Measured single ended into 50 Ω load.

Specifications subject to change without notice.
DEFINITIONS OF SPECIFICATIONS

Linearity Error (Also Called Integral Nonlinearity or INL)
Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (or DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A D/A converter is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
The deviation of the output current from the ideal of zero is called offset error. For IOUTA, 0 mA output is expected when the inputs are all 0s. For IOUTB, 0 mA output is expected when all inputs are set to 1s.

Gain Error
The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1s minus the output when all inputs are set to 0s.

Output Compliance Range
The range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (+25°C) value to the value at either T_MIN or T_MAX. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per °C. For reference drift, the drift is reported in ppm per °C.

Power Supply Rejection
The maximum change in the full-scale output as the supplies are varied from nominal to minimum and maximum specified voltages.

Settling Time
The time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

Glitch Impulse
Asymmetrical switching times in a DAC give rise to undesired output transients that are quantified by a glitch impulse. It is specified as the net area of the glitch in pV-s.

Spurious-Free Dynamic Range
The difference, in dB, between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Total Harmonic Distortion
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal. It is expressed as a percentage or in decibels (dB).

Multitone Power Ratio
The spurious-free dynamic range for an output containing multiple carrier tones of equal amplitude. It is measured as the difference between the rms amplitude of a carrier tone to the peak spurious signal in the region of a removed tone.

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Figure 2. Basic AC Characterization Test Setup

\[ I_{FS} = 32 I_{ref} \]
Typical AC Characterization Curves @ +5 V Supplies

(AVDD = +5 V, DVDD = +5 V, IOUTS = 20 mA, 50 Ω Doubly Terminated Load, Differential Output, TA = +25°C, SFDR up to Nyquist, unless otherwise noted)

Figure 3. SFDR vs. f_OUT @ 0 dBFS

Figure 4. SFDR vs. f_OUT @ 25 MSPS

Figure 5. SFDR vs. f_OUT @ 50 MSPS

Figure 6. SFDR vs. f_OUT @ 65 MSPS

Figure 7. SFDR vs. f_OUT @ 125 MSPS

Figure 8. SFDR vs. f_OUT and IOUTS @ 25 MSPS and 0 dBFS

Figure 9. Single-Tone SFDR vs. A_OUT @ f_OUT = f_CLOCK/11

Figure 10. Single-Tone SFDR vs. A_OUT @ f_OUT = f_CLOCK/5

Figure 11. SNR vs. f_CLOCK and IOUTS @ f_OUT = 2 MHz and 0 dBFS
Figure 12. Typical INL

Figure 13. Typical DNL

Figure 14. SFDR vs. Temperature @ 125 MSPS, 0 dBFS

Figure 15. Dual-Tone SFDR

Figure 16. Four-Tone SFDR

AVDD

current sources

switches
**FUNCTIONAL DESCRIPTION**

Figure 17 shows a simplified block diagram of the AD9752. The AD9752 consists of a large PMOS current source array that is capable of providing up to 20 mA of total current. The array is divided into 31 equal currents that make up the five most significant bits (MSBs). The next four bits or middle bits consist of 15 equal current sources whose value is 1/16th of an MSB current source. The remaining LSBs are binary weighted fractions of the middle-bits current sources. Implementing the middle and lower bits with current sources, instead of an R-2R ladder, enhances its dynamic performance for multitone or low amplitude signals and helps maintain the DAC's high output impedance (i.e., >100 kΩ).

All of these current sources are switched to one or the other of the two output nodes (i.e., IOUTA or IOUTB) via PMOS differential current switches. The switches are based on a new architecture that drastically improves distortion performance. This new switch architecture reduces various timing errors and provides matching complementary drive signals to the inputs of the differential current switches.

The analog and digital sections of the AD9752 have separate power supply inputs (i.e., AVDD and DVDD). The digital section, which is capable of operating up to a 125 MSPS clock rate and over a +2.7 V to +5.5 V operating range, consists of edge-triggered latches and segment decoding logic circuitry. The analog section, which can operate over a +4.5 V to +5.5 V range, includes the PMOS current sources, the associated differential switches, a 1.20 V bandgap voltage reference and a reference control amplifier.

The full-scale output current is regulated by the reference control amplifier and can be set from 2 mA to 20 mA via an external resistor, RSET. The external resistor, in combination with the reference control amplifier and voltage reference VREF0, sets the reference current IREF, which is mirrored over to the segmented current sources with the proper scaling factor. The full-scale current, IOUTFS, is thirty-two times the value of IREF.

**DAC TRANSFER FUNCTION**

The AD9752 provides complementary current outputs, IOUTA and IOUTB. IOUTA will provide a near full-scale current output, IOUTFS, when all bits are high (i.e., DTCODE = 4095) while IOUTB, the complementary output, provides no current. The current output appearing at IOUTA and IOUTB is a function of both the input code and IOUTFS and can be expressed as:

\[ IOUTA = (DAC CODE/4096) \times IOUTFS \]  

\[ IOUTB = (4095 - DAC CODE)/4096 \times IOUTFS \]

where DAC CODE = 0 to 4095 (i.e., Decimal Representation).

As mentioned previously, IOUTFS is a function of the reference current IREF, which is nominally set by a reference voltage VREF0 and external resistor RSET. It can be expressed as:

\[ IOUTFS = 32 \times IREF \]

where \[ IREF = \frac{VREF0}{RSET} \]

The two current outputs will typically drive a resistive load directly or via a transformer. If dc coupling is required, IOUTA and IOUTB should be directly connected to matching resistive loads, RLOAD, which are tied to analog common, ACOM. Note, RLOAD may represent the equivalent load resistance seen by IOUTA or IOUTB as would be the case in a doubly terminated 50 Ω or 75 Ω cable. The single-ended voltage output appearing at the IOUTA and IOUTB nodes is simply:

\[ VOUTA = IOUTA \times RLOAD \]

\[ VOUTB = IOUTB \times RLOAD \]

Note the full-scale value of VOUTA and VOUTB should not exceed the specified output compliance range to maintain specified distortion and linearity performance.

The differential voltage, VDIFF, appearing across IOUTA and IOUTB is:

\[ VDIFF = (IOUTA - IOUTB) \times RLOAD \]

Substituting the values of IOUTA, IOUTB, and IREF; VDIFF can be expressed as:

\[ VDIFF = \left( (2 \times DAC CODE) - 4095 \right) \times (32 \times \frac{RLOAD}{RSET}) \times VREF0 \]

These last two equations highlight some of the advantages of operating the AD9752 differentially. First, the differential operation will help cancel common-mode error sources associated with IOUTA and IOUTB such as noise, distortion and dc offsets. Second, the differential code dependent current and subsequent voltage, VDIFF, is twice the value of the single-ended voltage output (i.e., VOUTA or VOUTB), thus providing twice the signal power to the load.

Note, the gain drift temperature performance for a single-ended (VOUTA and VOUTB) or differential output (VDIFF) of the AD9752 can be enhanced by selecting temperature tracking resistors for RLOAD and RSET due to their ratiometric relationship as shown in Equation 8.
**AD9752**

![Figure 28. Differential Output Using a Transformer](image)

The center tap on the primary side of the transformer must be connected to ACOM to provide the necessary dc current path for both IOUTA and IOUTB. The complementary voltages appearing at IOUTA and IOUTB (i.e., VOUTA and VOUTB) swing symmetrically around ACOM and should be maintained with the specified output compliance range of the AD9752. A differential resistor, RDIFF, may be inserted in applications in which the output of the transformer is connected to the load, RL, via a passive reconstruction filter or cable. RDIFF is determined by the transformer's impedance ratio and provides the proper source termination which results in a low VSWR. Note that approximately half the signal power will be dissipated across RDIFF.

**DIFFERENTIAL USING AN OP AMP**

An op amp can also be used to perform a differential to single-ended conversion as shown in Figure 29. The AD9752 is configured with two equal load resistors, RL, of 25 Ω. The differential voltage developed across IOUTA and IOUTB is converted to a single-ended signal via the differential op amp configuration. An optional capacitor can be installed across IOUTA and IOUTB forming a real pole in a low-pass filter. The addition of this capacitor also enhances the op amp's distortion performance by preventing the DACs high slew rate output from overloading the op amp's input.

![Figure 29. DC Differential Coupling Using an Op Amp](image)

The common-mode rejection of this configuration is typically determined by the resistor matching. In this circuit, the differential op amp circuit is configured to provide some additional signal gain. The op amp must operate off of a dual supply since its output is approximately ±1.0 V. A high speed amplifier such as the AD8055 or AD9632 capable of preserving the differential performance of the AD9752 while meeting other system level objectives (i.e., cost, power) should be selected. The op amp differential gain, its gain setting resistor values, and full-scale output swing capabilities should all be considered when optimizing this circuit.

The differential circuit shown in Figure 30 provides the necessary level-shifting required in a single supply system. In this case, AVDD which is the positive analog supply for both the AD9752 and the op amp is also used to level-shift the differential output of the AD9752 to mid-supply (i.e., AVDD/2). The AD8041 is a suitable op amp for this application.

![Figure 30. Single-Supply DC Differential Coupled Circuit](image)

**SINGLE-ENDED UNBUFFERED VOLTAGE OUTPUT**

Figure 31 shows the AD9752 configured to provide a unipolar output range of approximately 0 V to +0.5 V for a doubly terminated 50 Ω cable since the nominal full-scale current, IOUTFS, of 20 mA flows through the equivalent RL of 25 Ω. In this case, RL represents the equivalent load resistance seen by IOUTA or IOUTB. The unused output (IOUTA or IOUTB) can be connected to ACOM directly or via a matching RL. Different values of IOUTFS and RL can be selected as long as the positive compliance range is adhered to. One additional consideration in this mode is the integral nonlinearity (INL) as discussed in the ANALOG OUTPUT section of this data sheet. For optimum INL performance, the single-ended, buffered voltage output configuration is suggested.

![Figure 31. 0 V to +0.5 V Unbuffered Voltage Output](image)

**SINGLE-ENDED, BUFFERED VOLTAGE OUTPUT CONFIGURATION**

Figure 32 shows a buffered single-ended output configuration in which the op amp U1 performs an I-V conversion on the AD9752 output current. U1 maintains IOUTA (or IOUTB) at a virtual ground, thus minimizing the nonlinear output impedance effect on the DAC's INL performance as discussed in the ANALOG OUTPUT section. Although this single-ended configuration typically provides the best dc linearity performance, its ac distortion performance at higher DAC update rates may be limited by U1's slew rate capabilities. U1 provides a negative unipolar output voltage and its full-scale output voltage is simply the product of IR and IOUTS. The full-scale output should be set within U1's voltage output swing capabilities by scaling IOUTS and/or IR. An improvement in ac distortion performance may result with a reduced IOUTS since the signal current U1 will be required to sink will be subsequently reduced.
POWER AND GROUNDING CONSIDERATIONS, POWER SUPPLY REJECTION

Many applications seek high speed and high performance under less than ideal operating conditions. In these circuits, the implementation and construction of the printed circuit board design is as important as the circuit design. Proper RF techniques must be used for device selection, placement and routing as well as power supply bypassing and grounding to ensure optimum performance. Figures 42-47 illustrate the recommended printed circuit board ground, power and signal plane layouts which are implemented on the AD9752 evaluation board.

One factor that can measurably affect system performance is the ability of the DAC output to reject dc variations or ac noise superimposed on the analog or digital dc power distribution (i.e., AVDD, DVDD). This is referred to as Power Supply Rejection Ratio (PSRR). For dc variations of the power supply, the resulting performance of the DAC directly corresponds to a gain error associated with the DAC's full-scale current, $I_{OUTFS}$. AC noise on the dc supplies is common in applications where the power distribution is generated by a switching power supply. Typically, switching power supply noise will occur over the spectrum from tens of kHz to several MHz. PSRR vs. frequency of the AD9752 AVDD supply, over this frequency range, is given in Figure 33.

![Figure 33. Power Supply Rejection Ratio of AD9752](image)

Note that the units in Figure 33 are given in units of (amps out)/(volts in). Noise on the analog power supply has the effect of modulating the internal switches, and therefore the output current. The voltage noise on the dc power, therefore, will be added in a nonlinear manner to the desired $I_{OUT}$. Due to the relative different sizes of these switches, PSRR is very code dependent. This can produce a mixing effect which can modulate low frequency power supply noise to higher frequencies. Worst case PSRR for either one of the differential DAC outputs will occur when the full-scale current is directed towards that output. As a result, the PSRR measurement in Figure 33 represents a worst case condition in which the digital inputs remain static and the full-scale output current of 20 mA is directed to the DAC output being measured.

An example serves to illustrate the effect of supply noise on the analog supply. Suppose a switching regulator with a switching frequency of 250 kHz produces 10 mV rms of noise and for simplicity sake (i.e., ignore harmonics), all of this noise is concentrated at 250 kHz. To calculate how much of this undesired noise will appear as current noise super imposed on the DAC’s full-scale current, $I_{OUTFS}$, one must determine the PSRR in dB using Figure 33 at 250 kHz. To calculate the PSRR for a given $R_{LOAD}$, such that the units of PSRR are converted from A/V to V/V, adjust the curve in Figure 33 by the scaling factor $20 \times \log (R_{LOAD})$. For instance, if $R_{LOAD}$ is 50 $\Omega$, the PSRR is reduced by 34 dB (i.e., PSRR of the DAC at 1 MHz which is 74 dB in Figure 33 becomes 40 dB $V_{OUT}/V_{IN}$).

Proper grounding and decoupling should be a primary objective in any high speed, high resolution system. The AD9752 features separate analog and digital supply and ground pins to optimize the management of analog and digital ground currents in a system. In general, AVDD, the analog supply, should be decoupled to ACOM, the analog common, as close to the chip as physically possible. Similarly, DVDD, the digital supply, should be decoupled to DCOM as close as physically possible.

For those applications that require a single +5 V or +3 V supply for both the analog and digital supply, a clean analog supply may be generated using the circuit shown in Figure 34. The circuit consists of a differential LC filter with separate power supply and return lines. Lower noise can be attained using low ESR type electrolytic and tantalum capacitors.

![Figure 34. Differential LC Filter for Single +5 V or +3 V Applications](image)

Maintaining low noise on power supplies and ground is critical to obtaining optimum results from the AD9752. If properly implemented, ground planes can perform a host of functions on high speed circuit boards: bypassing, shielding, current transport, etc. In mixed signal design, the analog and digital portions of the board should be distinct from each other, with the analog ground plane confined to the areas covering the analog signal traces, and the digital ground plane confined to areas covering the digital interconnects.

All analog ground pins of the DAC, reference and other analog components should be tied directly to the analog ground plane. The two ground planes should be connected by a path 1/8 to 1/4 inch wide underneath or within 1/2 inch of the DAC to