OUTLINE

- Software Tools
- Preliminary Calculations
- Mathematical Design Script, MATLAB
- Simulink Modeling
- Circuit Implementation
- Simulink Results
- Suggestions
SOFTWARE TOOLS

- MATLAB/Simulink
- Delta Sigma Toolbox (MATLAB)
  - http://www.mathworks.com/matlabcentral/fileexchange/19
- SD Toolbox 2 (Simulink)
- Cadence/Spectre
- SWITCAP (“sw2” on SunOS machine)
WHERE TO BEGIN

- Panic for 5 seconds...
- Now, Stop Panicking
- Examine Requirements
  + ENOB, $F_{BW}$, $F_S$, etc.
- Determine Target Technology
  + Same as ECE 626?
- Explore DStoolbox Demos
  + dsdemo[1-3,5].m
TRADEOFFS IN ΔΣ PARAMETERS

- Calculate SQNR
- Modulator Order, OSR, Quantizer Levels
- Power efficient designs → thermal noise limited, quantization noise limited
EMPERICAL SQNR LIMITS

- Compare Modulator Order vs. OSR vs. Quantizer Resolution

[Schreier and Temes, 2005]
Consider ΔΣ Topologies
- Single Loop vs. MASH; CIFB, CIFF, CRFB, CRFF, etc.

Write MATLAB script to optimize coefficients
- Order, OSR, Bits, \( \|H\|_\infty \), etc.
- DStoolbox → dsdemo[1-3].m
MATLAB SCRIPT OUTPUT

- Modulator Coefficients
- NTF and STF
  + Magnitude
  + Poles and Zeros
- Time-domain Simulation Results

**Modulator Coefficients**

<p>| | |</p>
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<tr>
<td>$a_1$</td>
<td>2.885522268923101</td>
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<td>$c_1$</td>
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<td>$g_1$</td>
<td>0.022954073145617</td>
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**Magnitude**

- Frequency (Hz)
- Magnitude (dB)

**Poles and Zeros**

- Real
- Imaginary

**Signal-to-Noise Ratio**

- Relative Signal Amplitude
- Signal-to-Noise Ratio
Refer to dsdemo3.m
scaleABCD( , , , [x₁, ..., x_L], , , )
xlim = [x₁, ..., x_L]
Iteratively adjust values of xlim to change [a, b, c, g] coefficients
Examine [a, b, c, g] coefficients for integer ratio quantization → Eases switched-capacitor integrator ratios, and matching
Maximize State Amplitude to minimize distortion

Leave some margin
FILTER DESIGN

- MATLAB fdatool
  - Multirate filter (CIC Decimator)
  - Design Post Filter
  - Quantize Coeff.
    - Fixed-point Math
- Export to Script or Simulink
Use as starting point

Noise Sources
+ kT/C Noise
+ White Noise

Real Integrator
+ Finite Gain
+ Gain Bandwidth
+ Slew Rate
- Finite Gain & BW, SR
- DAC & Cap Mismatch
- Analog Noise
- Digital Round-off Errors
- Create MATLAB script to control Simulink model
- Initialize variables in MATLAB script
- Choose “Accelerator” to speedup simulation
  - Must have C/C++
- Configuration Parameters → Solver options → variable step, discrete (no continuous states)
Folding of quantization error
Shifts NTF zero locations
SLEW RATE – SIMULINK

- Based on max integrator step size
- Abrupt impact on integrator settling
- Interdependence with GBW
Can cause increased in-band quantization noise

- GBW of the order of $F_S$
- Interdependence with Slew Rate
Examine dsdemo5.m
Mismatch causes distortion
DWA high-pass filters mismatch
MATLAB fdatool
Quantize Coeff.
Internal Precision
Output Fraction Bits
Code into MATLAB → Easier Testing
Includes non-ideal effects
- DWA active (8-bit matching)
- Average of 32 runs, $2^{16}$ points
  - Initialize Integrator States Randomly
ADC Spectrum

- PSD of Decimated and Filtered Output
- $F_{BW} = 20$ MHz

<table>
<thead>
<tr>
<th>Design Specifications</th>
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<tbody>
<tr>
<td>Signal Bandwidth</td>
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<tr>
<td>Clock Frequency</td>
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<tr>
<td>Min Unit Cap</td>
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<tr>
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<td>Amplifier DC Gain</td>
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<td>ENOB @ 156.25 kHz</td>
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<td>ENOB @ 20 MHz</td>
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<tr>
<td>Power Supply</td>
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<tr>
<td>Input Signal Range</td>
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PROJECT SUGGESTIONS

- **Start Early!**
- Understand DS Toolbox dsdemo’s
- Write DS Toolbox Script
  + *Fully* test before starting Simulink and Cadence!!!
- Build Transistor-based Switches in Cadence
  + Helps mitigate convergence issues
- Understand SD Toolbox 2 (Simulink) and adapt to your system