ECE 418/518
Semiconductor Device Processing

Ion Implantation
Ion Implantation

Typical applications in device processing

• As an alternative to diffusion (in particular pre-deposition) for the doping of semiconductors
• Threshold voltage control in MOS processing
• For the creation of buried oxide
• Creation of damage for device isolation and gettering of impurities
• To produce samples with an accurately known concentration of a given impurity as calibration standards for other measurements such as secondary ion mass spectroscopy (SIMS)

Main advantages of ion implantation

• Accurate control of dose
• Better control of doping profiles and junction depth
Ion Implantation
High Energy Accelerator

1. Ion Source
2. Mass Spectrometer
3. High-Voltage Accelerator (Up to 5 MeV)
4. Scanning System
5. Target Chamber
Implantation Process

• Produce ions of a given impurity, accelerate to a high voltage and shoot the ions into the silicon sample.

• Ions travel almost along straight lines until they lose most of their energy. Then they undergo some collisions with the host lattice atoms before they come to rest.

• The mean distance they travel before they come to rest is known as the projected range.

• Since the collision of ions is a statistical process, some ions travel more depth while the others travel less distance than the mean projected range. The spread of the ion range is known as the straggle.

• The implanted profile is a Gaussian according to the theory of Lindhard, Scharff and Schiott (LSS).

• The projected range is proportional to the acceleration voltage. Integrated dose is given by the product of the ion current and the duration.
Ion Implantation
Mathematical Model

Gaussian Profile

\[ N(x) = N_p \exp \left[ - \frac{(x - R_p)^2}{2\Delta R_p^2} \right] \]

- \( R_p \) = Projected Range
- \( \Delta R_p \) = Straggle

Dose \( Q = \int_0^\infty N(x)dx = \sqrt{2\pi N_p \Delta R_p} \)
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Projected Range and Straggle

(a)

(b)
Selective implantation

• Photoresist, oxide or nitride is used as a masking layer for selective implantation. The thickness of the masking layer should be made greater than the projected range of the desired impurity in the masking material for the given acceleration voltage used.

• Example:

Selective implantation is used in the self-aligned process in the fabrication of MOS transistors. Source/drain implantation is done using poly-silicon gate as the mask.

The lateral spread of the implanted profile under the masked area is given by the straggle parameter.
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Selective Implantation

\[ N(x,y) = N(x)F(y) \]

\[ F(y) = \frac{1}{2} \left[ \text{erfc} \left( \frac{y - a}{\sqrt{2\Delta R_{\perp}}} \right) - \text{erfc} \left( \frac{y + a}{\sqrt{2\Delta R_{\perp}}} \right) \right] \]

\[ \Delta R_{\perp} = \text{transverse straggle} \]

\( N(x) \) is one-dimensional solution

Contours of equal ion concentration for an implantation into silicon through a 1-\( \mu \)m window. The profiles are symmetrical about the x-axis and were calculated using the equation above taken from Ref. [3].
Post-implant annealing

Post-implant annealing at a high temperature (> 800 °C) is necessary for the following two reasons.

1. To anneal the damage suffered by the host lattice during the implantation process.

2. To activate the impurities - the implanted impurity species may not come to rest at a (substitutional) lattice site. The annealing process helps the impurity atoms move around and occupy the lattice sites. The impurities become electrically active only after they occupy the lattice sites.

If the implantation process is followed by a drive-in or an oxidation process, then that process also serves the purpose of annealing. If a drive-in process is not required, then an annealing at a temperature of 800 - 900 °C in a nitrogen atmosphere is carried out.

Two different forms of annealing are used:

1. Conventional furnace annealing.

2. Rapid Thermal Annealing - Quartz halogen lamps are used to heat the silicon wafer at a rapid rate. The annealing is usually done within 5 -10 seconds. Helpful in reducing the overall thermal budget of the wafer.
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High dose implant

FIGURE 5.9
A plot of the dose required to form an amorphous layer on silicon versus reciprocal target temperature. Arsenic falls between phosphorus and antimony. Copyright 1970 by Plenum Publishing Corporation. Reprinted with permission from Ref. [6].
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Rapid Thermal Annealing

Figure 5.12
(a) Concept for a rapid thermal annealing (RTP) system. (b) Applied Materials 300 mm RTP System (Courtesy Applied Materials)

• Rapid Heating
• 950-1050°C
• 50°C/sec
• Very Low Dt
Shallow Implantation

• Modern VLSI processes require very shallow (~ 20 nm) source/drain junctions
• Very high doses are also required to keep the sheet resistance low
• New processes using very low energy ions had to be invented
• New sources with heavy masses (e.g. decaborane $\text{B}_{10}\text{H}_{14}$) also had to be developed
• A new unusual phenomenon known as Transient Enhanced Diffusion was discovered which distorts the impurity profile considerably
  • Enhancement of diffusion by the local damage is known as Transient Enhanced Diffusion.
  • The effect disappears as soon as the damage is annealed out
Channeling

• When the implantation is done in single crystals, if the beam is exactly aligned to a crystallographic direction, then the beam will travel much deeper into the crystal than the projected range given by the LSS theory. This phenomenon is known as channeling.

• During semiconductor processing, care must be taken to avoid channeling. This is done by deliberately misaligning the beam slightly (by about 5-10°) from the exact crystallographic direction.

• Channeling of alpha particles is used to monitor residual implantation damage after annealing and in the determination of the lattice location of the impurities.
Ion Implantation
Channeling

FIGURE 5.7
The silicon lattice viewed along the [110] axis. From THE ARCHITECTURE OF MOLECULES by Linus Pauling and Roger Hayward. Copyright © 1964 W. H. Freeman and Company. Reprinted with permission from Refs. [4a] and [4b].

FIGURE 5.8
Phosphorus impurity profiles for 40-keV implantations at various angles from the axis. Copyright 1968 by national Research Council of Canada. Reprinted with permission from Ref. [5].