General Course Information

- **Instructor:** Mani Sivaramakrishnan, School of EECS
  
  Office Room #: KEC  
  Office Hours: By appointment  
  Phone:  
  E-mail: sivarams@engr.orst.edu  
  Class web page:  
  [http://classes.engr.oregonstate.edu/eecs/spring2017/ece418-001/](http://classes.engr.oregonstate.edu/eecs/spring2017/ece418-001/)

- Class hours: WF: 16:00 – 17:50  
  Kidder 200

- Laboratory: To be arranged

- **Textbook:** *Introduction to Microelectronics Fabrication, 2nd Edn.*  
  - Purdue Modular Series on Solid State Devices, vol. V  
  - Author: Richard Jaeger (Prentice-Hall Publishing, 2002)
Course outline

- Week 1 – Introduction, processing overview
- Week 2 – Oxidation and SUPREM process modeling
- Week 3 – Diffusion and characterization
- Week 4 – Ion implantation and photolithography
- Weeks 5 - Deposition and etch
- Week 6 to 9 – MOS and Bipolar process integration

**Grading:**
- Labwork 50% (Experiment #1 MOS capacitors: 15%)
  - (Experiment #2 NMOS transistors plus SUPREM modeling 35%)
- Homework assignments 20%
- Midterm Exam – 15% (Week 7)
- Project – 15%

**No final examination**
Course Objectives

- Classroom instruction:
  - Learn the theory of integrated circuit (IC) manufacturing technology.
    - Silicon CMOS and Bipolar technology – *we will do only NMOS in lab*
    - Overview of different unit processes (oxidation, lithography, diffusion, deposition, etching, etc.) and process integration.
    - Process (and device) modeling using SUPREM (and ATLAS).

- Laboratory instruction:
  - Actual hands-on experience in the fabrication and characterization of MOS capacitors and NMOS transistors. (The level of technology in the lab is a bit crude and several generations behind the current industry standards. Nevertheless, it is adequate to learn about the technology and to prepare you for work in the semiconductor processing industry.)
Laboratory sessions

- Lab Manual and safety:
  - (Will be) Available on the web. The rules and the guidelines are for your safety. Read the manual carefully. The rules should be observed very strictly. No violations please! **We will not compromise on lab safety.** Electrical, chemical and fire hazards are real. Please do not ignore them.

- Lab records:
  - 2 (or 3) member groups. Emphasis on team work. One report per group for each project. **Record all your predictions, lab data, observations, comments and thoughts in your lab notebook.** Date each day, write legibly so others can read and understand.

- T.A.s:
  - Please ask questions as they come up. The laboratory work is a major component of learning in this class.
Evolution of Microelectronics Technology

- **Wafer diameter:**
  - Currently 300 mm (12”) diameter wafers are used by many leading chip manufacturers and 200 mm (8”) wafers by a majority of lower volume companies. Transition to 450 mm expected 2020 – 2025 timeframe.

- **Maximum die size:** ~ 25 mm x 25 mm

- **Lithography (or minimum feature size)**
  - Smallest 10 nm; Quite a few fabs can do 10 – 45 nm; 45 nm and above by many leading manufacturers;
  - Multilevel interconnects, low k dielectrics
  - Currently up to 10 levels of interconnect metal are used to realize the complex circuits. Copper as interconnect metal.

- **Chemical mechanical polishing (CMP):** planarization technique.
Evolution of Microelectronics Technology

Silicon wafers – 2” to 12”

Intel Pentium 4 processor
(Die size: 24 mm x 25 mm)
Evolution of Device Complexity

- First transistor: 1947 (Shockley, Bardeen, Brattain; Bell Labs)
World’s First Integrated Circuits (ICs)

1958 Texas Instruments – first ever
   Jack Kilby

1960 Fairchild Semiconductor
   Bob Noyce
   First monolithic, planar IC
Growth of Silicon Single Crystals

Czochralski Growth

Float Zone Growth
Czochralski Crystal Growth
Silicon (Si) Properties

- High quality native oxide
- Diamond cubic crystal structure – 2 fcc lattices offset by \( \frac{1}{4} \) of a body diagonal of unit cell
- Every Si atom has 4 nearest neighbor atoms
- Main crystal planes [100], [110], [111]
- Different atomic densities on each plane – controls many processing properties
- \( a = 5.43 \text{ Å} = \text{lattice constant} = \text{unit cell edge} \)
Silicon ingot to wafers

As-grown crystal ingot

Grind crystal to a smooth finish and grind orientation flat.

Saw into thin slices or wafers

Grind the edge to a smooth round finish

Lap and polish slice
MOS Capacitor and NMOS Transistor

MOS Capacitor

NMOS Transistor

V_G

Oxide

Metal

Semiconductor

p-substrate

n-channel

deployment region

S

D

n+

G

V_{GS}

V_{DS}

B

Mani S. ECE 418/518 Spring 2017