ECE 418/518 Semiconductor Device Processing, Spring 2017

Oxide Characterization
Important oxide properties to be characterized

• Oxide thickness
  › Estimation (calculation) from the process parameters
  › From the color of the oxide film (See Table 3.2, p.44, R.C. Jaeger)
  › Ellipsometry

• Defects in the oxide
  › Fixed Charges
  › Mobile ions
  › Oxide traps
  › Interface traps
  All the above types of defects can be characterized by using C-V measurements of MOS capacitor.

• Dielectric Breakdown strength
Oxide Thickness Characterization: Ellipsometer
Ellipsometry

Snell’s Law: \( n_i \sin \theta_i = n_t \sin \theta_t \)

Fresnel Reflection:

\[
\begin{align*}
    r_p &= \frac{E_{rp}}{E_{ip}} = \frac{n_t \cos \theta_i - n_i \cos \theta_t}{n_t \cos \theta_i + n_i \cos \theta_t} \\
    t_p &= \frac{E_{rp}}{E_{ip}} = \frac{2n_i \cos \theta_i}{n_t \cos \theta_i + n_i \cos \theta_t} \\
    r_s &= \frac{E_{rs}}{E_{is}} = \frac{n_i \cos \theta_i - n_t \cos \theta_t}{n_i \cos \theta_i + n_t \cos \theta_t} \\
    t_s &= \frac{E_{ts}}{E_{is}} = \frac{2n_i \cos \theta_i}{n_i \cos \theta_i + n_t \cos \theta_t}
\end{align*}
\]
Figure 2-5. If linearly polarized light makes a reflection, the resultant light is elliptically polarized. Conceptually, the QWP could change it back to linearly polarized light and the analyzer could find a null. The angular settings of the QWP and the analyzer could be used to determine the phase shift and attenuation ratio. This is a conceptual use of these elements. Actual practice is somewhat different.
Ellipsometry (schematic - actual)

Figure 2-8. In actual practice of null ellipsometry, the QWP is placed before the reflection and is held in a fixed position. The polarizer and analyzer are rotated to find the null.
MOS capacitor characterization

- Ideal MOS C-V curves ($V_{FB} = 0$)
  - Accumulation
  - Depletion
  - Inversion
- Low frequency and high frequency C-V curves
- Flat band capacitance
- Threshold voltage
- Real MOS C-V curves
  - Nonzero flat band voltage $V_{FB}$ due to the defects in the oxide and the metal-semiconductor work function difference
- Characterization of oxide charges
Ideal MOS C-V curves

*LF*: Inversion charge is able to follow the dc bias and the ac probe voltage

*HF*: Inversion charge is able to follow the dc bias but not the ac probe voltage

*DD*: No inversion charge; non-equilibrium; electron-hole pairs are generated
Flat band capacitance

- Flat band conditions - No band bending in the semiconductor. Note that the Fermi levels in the metal and in the semiconductor, $E_{FM}$ and $E_{FS}$ are aligned at zero bias.
  - For an ideal MOS, $V_{FB} = 0$
  - Under flat band conditions the semiconductor capacitance $C_s = $ Debye length capacitance
  - Debye length $L_D = \left\{K_s\varepsilon_0kT/(q^2N_A)\right\}^{1/2}$
- Flat band capacitance $C_{FB}$ is a series combination of oxide capacitance and the Debye length capacitance.
- $C_{FB} = \left[ 1/C_{ox} + 1/C_s \right]^{-1} = \left[ d_{ox} / (K_{ox}\varepsilon_0) + L_D / (K_s\varepsilon_0) \right]^{-1}$
- Normalized flat band capacitance $C_{FB} / C_{ox} = \left[ 1 + (K_{ox}/K_s) \left( L_D / d_{ox} \right) \right]^{-1}$
Threshold voltage

- \( V_{\text{TH}} = \text{Gate (metal) voltage at which } V_{\text{si}} = 2\phi_F \)
  - \( \phi_F = E_i - E_F = (kT/q) \ln (p/n_i) \)
- At \( V_{\text{TH}} \) the depletion width reaches a maximum:
  - \( W_{\text{max}} = \{2K_s\varepsilon_02\phi_F/(qN_A)\}^{1/2} \)
- \( V_{\text{TH}} = V_{\text{ox}} \text{ (at } 2\phi_F) + 2\phi_F \)
  - \( = Q_{\text{depl}}/C_{\text{ox}} + 2\phi_F \)
  - \( = qN_A W_{\text{max}} t_{\text{ox}}/(K_{\text{ox}}\varepsilon_0) + 2\phi_F \)
- For real MOS, we need to add the flat band voltage (due to the non-idealities of the MOS capacitor metal-semiconductor work function difference and any contribution from oxide charges)
  - \( V_{\text{TH}} = V_{\text{FB}} + qN_A W_{\text{max}} t_{\text{ox}}/(K_{\text{ox}}\varepsilon_0) + 2\phi_F \)
- \( V_{\text{FB}} = \phi_{\text{ms}} - Q_{\text{ox}} / C_{\text{ox}} \text{ (see next slide)} \)
Real MOS C-V curves

- Non-zero flat band voltage due to
  1. $\phi_{ms} = \phi_m - \phi_s \neq 0$ and
  2. Defects / charges in the oxide
- The true C-V curve shifts rigidly toward negative or positive voltage with respect to the ideal MOS C-V curve depending on whether the oxide charge is negative or positive, respectively.
  It is convenient to measure the shift of the C-V curve at $C_{FB}$.
  $$V_{FB} = \phi_{ms} - Q_{ox} / C_{ox}$$
Defects in Thermal SiO$_2$

- (1) Interface Trapped charge ($Q_{it}$) - located right at the interface. Changes charge state with applied bias. Causes a distortion of the C-V curve. Difficult to characterize.
- (2) Fixed Charge ($Q_f$) - Caused by the transition region between Si and SiO$_2$. Does not change charge state with applied bias. Causes a rigid shift of the C-V curve along the voltage axis.
- (3) Oxide Trapped charge ($Q_{ot}$) - Caused by the charge trapped in the oxide due to ionizing radiation. Causes a rigid shift of the C-V curve.
- (4) Mobile ion charge ($Q_m$) - Caused by alkali ions. These charges drift by the bias applied to the device during the device operation.
Characterization of fixed charges

- Fixed charges:
  - Located very close to the interface (< 30 Å).
  - Caused by the transition region between Si and SiO₂.
  - Depends upon the oxidation / annealing conditions and Si crystal orientation.

- Apply a -ve bias stress to move the mobile ions to the metal-oxide interface. Measure C-V. Compare the measured C-V curve with the ideal MOS C-V curve.

  Read flat band voltage $V_{FB}$.

  $$V_{FB} = \phi_{ms} - Q_f / C_{ox}$$

  $$Q_f = - C_{ox} (V_{FB} - \phi_{ms})$$
Characterization of mobile ions and oxide traps

• Mobile ions:
  › Caused by the contamination due to Na⁺, K⁺ and Li⁺ ions during processing. These ions drift inside the oxide during the device operation due to bias and thermal stress and cause device failures.

• Characterization of mobile ions: Heat the sample to ~ 200 °C and apply a positive voltage stress (typically 1 V/100A) for about 10 minutes and cool the sample under bias. Remove the bias stress and measure C-V. Repeat the experiment after applying a -ve voltage stress at ~ 200 °C for about 10 minutes. Measure ΔV_{FB}.
  › Q_m = - C_{ox} ΔV_{FB}

• Oxide traps:
  › More difficult to determine their exact spatial location inside the oxide. Depending upon their physical position, their influence on V_{FB} varies - maximum when located close to the oxide-semiconductor interface and minimum for the other interface.