Lecture 15
MOS Capacitors 2
Schroder: Chapters 2, 6

Announcements

Homework 3/6:
• Is online now.
• Due Today.
• I will return it next Monday (21st May).

Homework 4/6:
• Will be online later today.
• Due Monday May 21st at 10:00am.
• I will return it the following Monday (28th May).
Last Time

- On Friday we covered basics of capacitors.

- We covered the different regimes:
  - $C_{ox}$
  - $C_{-inv}$
  - $C_{flatband}$
  - Accumulation
  - Depletion
  - Inversion

$V$

$$\begin{align*}
\text{Normal} & \quad \text{Normal} & \quad \text{Electrolytic} & \quad \text{Variable}
\end{align*}$$
Last Time

- CV characteristics are in reality quite complex.
- Inversion is observable at low frequencies:

![Diagram showing CV characteristics](image)

Last Time

- We also discuss how we can also get rigid shifts in flatband voltage:

![Diagram showing flatband voltage shifts](image)
Last Time

- Where a variety of charges are present in an MOS capacitor:

![Diagram of MOS capacitor with various charges](image)

Mobile ionic charge

Fixed oxide charge

Interface trapped charge

Trapped oxide charge

SiO₂

silicon

Last Time

- We also talked about ionic motion:

![Graph of AC voltage and time](image)

\[ V_{AC} (\text{mV}) \]

\[ \text{Time (ms)} \]

\[ C \]

\[ V \]

\[ C_{ox} \]

\[ T = 250° \text{C} \]

HF

LF
Lecture 15

• Interface Trap Non-idealities.
• Quasistatic Capacitance Analysis.
• Conductance Method.
Interface Trap Non-idealities

- The unique characteristic of interface states is that they distort the shape of a $C-V$ curve, in one of several ways:

  ![Diagram showing $C-V$ curves with and without interface states](image)

- We typically employ **Quasistatic Method** to assess the interface state density.
  - This method relies on measuring and comparing low- and high-frequency $CV$ curves.
  - We use equivalent circuit models to describe the behavior.
  - Schroder covers all these equivalent circuits in a lot more detail if you are interested on p323.
**Equivalent Circuits**

**Low-frequency**

Capacitance due to interface charge

\[ C_{ox} \]

\[ C_s(V) \]

\[ C_{it}(V) \]

**High-frequency**

Oxide capacitance

Semiconductor capacitance

\[ C_{ox} \]

\[ C_s(V) \]

- These two equivalent circuits differ only by whether or not the interface states are able to follow the applied AC voltage.
- Thus, differences between these two curves are ascribed to interface states.

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**CV-Characteristics**

- Frequency-dispersion of the measured capacitance with respect to the applied AC voltage is used to assess the interface state density.

\[ C = \frac{Q}{\Delta V} \]

- The area indicated is a charge (since \( Q = CV \)).
  - We will come back to why this is useful.
Trapped Charge Density

- We define the interface charge density as follows:

\[ D_{it} = \frac{C_{it}}{qA} \]

Units of cm\(^2\) eV\(^{-1}\)

- Knowing that the only difference between the low frequency and high-frequency equivalent circuits is the presence of \(C_{it}\), we can deduce:

\[ D_{it} = \frac{1}{qA} \left[ \frac{C_{LF}C_{ox}}{C_{ox} - C_{LF}} - \frac{C_{HF}C_{ox}}{C_{ox} - C_{HF}} \right] \]

Surface Potential

- Note that \(D_{it}\) is evaluated in this manner as a function of voltage in order to obtain the interface state distribution.

- The area enclosed by the inside portion of the low-frequency \(CV\) curve is a measure of the surface potential modulation.

- This can be quantified by the Berglund Integral:

\[ \phi_s = \int_{V_1}^{V_2} \left( 1 - \frac{C_{LF}(V)}{C_{ox}(V)} \right) dV + \Delta \]

- \(\Delta\) is an integration constant.
Surface Potential

\[ \phi_s = \int_{V_1}^{V_2} \left( 1 - \frac{C_{LF}(V)}{C_{ox}(V)} \right) dV + \Delta \]

- To evaluate \( \Delta \), and therefore \( \phi_s \), we need to evaluate the surface potential to at one specific voltage.
- \( D_{it} \) is usually plotted as a function of \( \phi_s \):

Quasistatic Capacitance Analysis
Quasistatic Analysis

• Recall that our approach for measuring capacitance is to first apply a small-signal AC voltage and a DC voltage ramp, and to then evaluate capacitance as the change in charge responding to the AC voltage,

\[ V_{DC} \]
\[ t(s) \]

-10
-5
0
5
10

VAC (mV)
Time (ms)

Quasistatic Analysis

• In contrast, quasistatic approaches involve measuring either a current or charge, and then relating these to capacitance, if necessary.

• The motivation for quasistatic analysis is associated with the difficulty of measuring small-signal dynamic capacitances at low frequencies.
Quasistatic Analysis

- A common circuit used for quasistatic analysis is shown below:

![Quasistatic Analysis Diagram]

- The triangular component is an operational amplifier (Op-Amp).
- Basically, it provides an amplified signal proportional to the difference between the voltage at the "-" and "+") terminals.

Quasistatic Analysis

- Apply a linear voltage ramp:

\[
\frac{dV}{dt} = \alpha
\]

- In this case we can say:

\[
V_{out}(t) = -CR \frac{dV_{out}(t)}{dt} = -CR\alpha
\]
Quasistatic Analysis

- The total MOS capacitance is equal to:
  \[ C = -\frac{V_{out}}{R\alpha} \]

- Note that the quasistatic ‘frequency’ corresponds to the period of the DC ramp.
  - This can be quite slow, and can often be approximated as DC.
  - For example, if you cycled the gate voltage between ±5 V at a ramp rate of 10 mV/s, this would correspond to a quasistatic ‘frequency’ of \( 5 \times 10^{-4} \) Hz.

Displacement Current

- Another perspective on quasistatic analysis, which is sometimes quite useful, is to recognize that when a changing voltage is applied to a capacitor in the previously shown op-amp circuit, a displacement current flows across the feedback resistor.

- The displacement current is equal to:
  \[ I = C \frac{dV}{dt} \]

- The MOS capacitance is therefore:
  \[ C = \frac{I}{\frac{dV}{dt}} = \frac{I}{\alpha} \]
Differentiator Amplifiers

• One distinct disadvantage of the quasistatic op-amp circuit shown previously is that it is a differentiator, which means that it amplifies noise.

\[ f(t) \]
\[ \frac{df(t)}{dt} \]

• If you have a choice, it is best to avoid differentiators when doing characterization if the signal-to-noise ratio is problematic.

Integrator Amplifiers

• An alternative circuit is:

\[ V_{in} \]
\[ c \]
\[ C_F \]
\[ V_{out} \]

• Those familiar with circuits will recognize this as an integrator.
• Integrators are preferred for their low-pass filter, and hence noise-reduction.

See Schroeder p332-333 for more details
Integrator Amplifiers

• This type of amplifier would have the following effect:

\[ f(t) \]
\[ \int f(t) \, dt \]

• Since the inverting op-amp terminal is at virtual ground, the displacement current flowing in the MOS capacitor must be equal to the negative of that flowing through the feedback capacitor.

• This is a feature of an op-amp.

Integrator Amplifiers

• If the input voltage waveform consists of a series of voltage steps of magnitude \( \Delta V \), and if the switch shown in the op-amp circuit is closed between voltage steps to discharge the feedback capacitor, we can represent one voltage step as

\[ V_{IN}(t) = \Delta V u(t) \]

• Where \( u(t) \) is a step function.
Integrator Amplifiers

\[ V_{IN}(t) = \Delta V u(t) \]

- Taking the time derivative of this equation leads to:
  \[ \frac{dV_{IN}(t)}{dt} = \Delta V \delta(t) \]

- Where \( \delta(t) \) is a delta function
- We can combine this derivative with our equation for displacement current to get the capacitance of our MOS capacitor.

Integrator Amplifiers

- It turns out, that in this circuit configuration, the capacitance of our MOS capacitor is equal to:
  \[ C = -C_F \frac{\Delta V_{out}}{\Delta V} \]

- \( C \): Capacitance of the MOS capacitor we are testing.
- \( C_F \): Capacitance of feedback capacitor (user chosen).
- \( \Delta V_{out} \): Change in voltage measured due to step in input voltage.
- \( \Delta V \): Size of input voltage step.
Integrator Amplifiers

- It turns out, that in this circuit configuration, the capacitance of our MOS capacitor is equal to:
  \[ C = -C_F \frac{\Delta V_{out}}{\Delta V} \]

- This equation says that the MOS capacitance is given by the output voltage of the op-amp circuit.

- Moreover, the gain of this circuit can be controlled by choice of the feedback capacitance \( C_F \).

- The change in charge across the MOS capacitor is:
  \[ \Delta Q = C \Delta V = -C_F \Delta V_{out} \]

Conductance Method
Conductance Method

- The conductance method is the most sensitive and comprehensive method for measuring interface states, providing a sensitivity of $10^9 \text{ cm}^{-2} \text{ eV}^{-1}$ as well as information on the capture cross sections for majority carriers and surface potential fluctuations.
  - $10^9 \text{ cm}^{-2} \text{ eV}^{-1}$ is very sensitive.
  - However, it is very time-intensive technique.
  - The equivalent circuits shown on the next page elucidate the basic idea behind the conductance method.

Interface Trapped Charge

- Recall, last lecture we talked about interface trapped charge.
Physical Equivalent Circuit

- We can describe the circuit as shown on the right.
- $C_{it}$ is the capacitance associated with interface trapped charge.
- $R_{it}$ is the resistance associated with interface trapped charge.
- Physically, $C_{it}$ represents charge storage, whereas $R_{it}$ accounts for energy dissipation associated with trap capture and emission.

Measured Circuit

- In reality we would only be able to measure total capacitance ($C_m$) and conductance ($G_m$).
- In the conductance method, $C_m$ and $G_m$ are measured as a function of voltage at a given AC frequency.
- This procedure is repeated at a large number of frequencies.
Conductance Data

- $C_m$ and $G_m$ plotted as a function of voltage for two different frequencies may look something like the following.

- Note that there is significantly more conductance than capacitance frequency-dispersion.

Parallel Circuit

- From the $(C_m) \text{ vs } V$ curve, we can evaluate the oxide capacitance ($C_{ox}$).

- With this knowledge, and the measured capacitance and conductance at a particular applied voltage, we can determine the “parallel” conductance.
Parallel Circuit

• For a particular applied voltage we can say the parallel capacitance is:

\[
\frac{G_p}{\omega} = \frac{\omega G_p G_{ox}^2}{G_m^2 + \omega^2 (G_{ox} - G_m)^2}
\]

• \(G_p\) is the conductance in the parallel model.
• \(\omega\) is the angular frequency (\(\omega = 2\pi f\)).
• \(G_m\) is the measured conductance.
• \(C_{ox}\) is the oxide capacitance.
• \(C_m\) is the measured capacitance.

Parallel Circuit

• Plotting parallel capacitance (normalised for angular frequency) as a function of voltage:

\[
\frac{G_p}{\omega} \quad \text{log}(\omega)
\]

• The interface state density \((D_{it})\) is then given by:

\[
D_{it} = \left| \frac{G_p}{\omega} \right|_{\text{max}} \frac{1}{q F_D} \quad \text{Correction factor} \sim 0.1-0.4
\]
Next Time

• Field Effect Transistors (FETs) Part 1.

\[ V = \pm \]

\[ I_{DS} \]

\[ V_{DS} \]