Lecture 16
Field-Effect Transistors 1
Schroder: Chapters 2, 4, 6

Announcements

Homework 4/6:
• Is online now.
• Due Monday May 21st at 10:00am.
• I will return it the following Monday (28th May).
Other Sources of Information

- It turns out that the information on FETs in Schroder is not well organized. It is spread across multiple chapters.
- There are some other good sources of information on this subject if you are interested:
  - Review Articles:
    - https://pubs.acs.org/doi/abs/10.1021/cr0501543
    - https://pubs.acs.org/doi/abs/10.1021/cm049391x
  - Books:
  - Course
    - ECE599 – Thin Film Electronics, John Labram, Fall 2018.

Lecture 16

- Introduction to Transistors.
- Operating Principles of FETs.
- Carrier Types.
- Combining Transistors.
Introduction to Transistors

What is a Transistor?

• 3-Terminal Electronic switch.
• Generally two symbols are used.
• Used to control flow of current between two terminals via a third terminal.

We will focus on FETs

Bipolar Junction Transistor

Field-Effect Transistor (FET)
The First Transistor

- Germanium was used in first transistor.
- Bardeen Brattain Shockley in 1947.[1]
- Bell labs.


Modern IC Development

Sand to Ingot  Wafer Dicing

https://www.youtube.com/watch?v=d9SWNLZvA8g
Modern IC Development

Photolithography  Ion Implantation

https://www.youtube.com/watch?v=d9SWNLZvA8g

Modern IC Development

Etching  Deposition

https://www.youtube.com/watch?v=d9SWNLZvA8g
Modern IC Development

Electrodeposition → CMP

https://www.youtube.com/watch?v=d9SWNLZvA8g

Modern IC Development

Circuit Design → Packaging

https://www.youtube.com/watch?v=d9SWNLZvA8g
Moore’s Law

- Suggested in the 1960’s by Intel’s founder George Moore.
- The number of transistors that can inexpensively fit onto a single integrated circuit will double every 24 months.\[1\]
- Today transistors can be purchased at a cost of $10^{-7}$ USD/transistor when part of integrated circuit.


Moore’s Law

- Remarkably, it has held up for 40 years.
Moore’s Law

- This has been driven by reducing feature size:

![Interconnects](image)

Size of the Industry

- Top 10 Semiconductor Vendors by Revenue, Worldwide, 2015 (Millions of Dollars):

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<td>153,182</td>
<td>-3</td>
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<td></td>
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<td>333,718</td>
<td>-1.9</td>
<td>100</td>
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http://www.gartner.com/newsroom/id/3182843
Operating Principles of FETs

Water Analogy

• Consider an analogy of water flowing in pipes.

[Diagram showing water analogy with nodes labeled Source, Drain, Flow Meter, Gate, Source-Drain Flow, Gate Pressure]
Water Analogy

- Consider an analogy of water flowing in pipes.

![Diagram of water analogy with labels: Source, Drain, Flow Meter, Gate, Pressure, and Flow Drain.]

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Spring 2018 - John Labram

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Water Analogy

• Consider an analogy of water flowing in pipes.

Source - Drain Flow
Gate Pressure
Flow Meter

Source

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Electrical Behavior

- A transistor can be considered to behave in a similar way:

![Diagram of transistor with labels for Gate Voltage, Drain Voltage, and Source-Drain Current.]}
Electrical Behavior

• A transistor can be considered to behave in a similar way:

Gate Voltage

Drain Voltage

Source-Drain Current

Gate Voltage

Ammeter

Electrical Behavior

• A transistor can be considered to behave in a similar way:

Gate Voltage

Drain Voltage

Source-Drain Current

Gate Voltage

Ammeter
Electrical Behavior

- Real transistors do not show this ideal behavior in reality:

![Graph showing the relationship between gate voltage and drain current for two different drain voltages.]

Structure of FETs

- A field effect transistor (FET) consists of three metal terminals, a semiconducting channel and a insulating dielectric.

- Source (S) and drain (D) electrodes are (normally) symmetric and in direct contact with the semiconducting channel.

- Insulating dielectric separates semiconductor from 3rd (gate) terminal.
Structure of FETs

- A wide range of FET structures exist.

**Bottom-Gate, Top-Contact**
- semiconductor
- dielectric
- metal (gate)

**Bottom-Gate, Bottom-Contact**
- semiconductor
- dielectric
- metal (gate)

**Top-Gate, Bottom-Contact**
- dielectric
- metal (gate)
- substrate (insulator)

Notice no dielectric

Structure of FETs

- A wide range of FET structures exist.

**MESFET**
- gate
- semiconductor
- substrate (insulator)

**Inversion mode FETs**
- gate
- semiconductor
- substrate (insulator)

**Fin-FETs**
- gate
- semiconductor
- substrate (insulator)
Operating Principles of FETs

- For our purposes we will consider a Bottom-Gate, Top-Contact FET.
- The principles discussed are general.
- As are the models we discuss next lecture.

Typically source electrode is grounded, voltages are applied to the drain and gate electrodes.
Operating Principles of FETs

- First, let’s consider structure under source electrode.

![Diagram showing the structure of a FET with labels for source, drain, semiconductor, dielectric, and gate.]

Conduction Band

Valence Band

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Operating Principles of FETs

• First, let’s consider the structure under the source electrode.

Conduction Band

Valence Band

Source

Semiconductor

Dielectric

Metal

$eV_G$

$+$V_G

Operating Principles of FETs

• Typically, the source electrode is grounded, voltages are applied to the drain and gate electrodes.
Operating Principles of FETs
• Application of gate voltage leads to injection of electrons into semiconductor, increasing conductivity.

Operating Principles of FETs
• Application of drain voltage then leads to a flow of electrons between the source and drain electrodes.
Operating Principles of FETs

• As $V_D$ increases relative to $V_G$, the field rotates and the distribution of accumulated charges changes.

Operating Principles of FETs

• As the distribution becomes inhomogeneous, relationship between $I_D$ and $V_D$ becomes non-linear.
Operating Principles of FETs

• Eventually channel becomes “pinched off” and no carriers are present adjacent to drain electrode.

This region has very high resistance

Source-Drain Current ($I_D$) vs Drain Voltage ($V_D$)

Operating Principles of FETs

• Pinched-off point moves towards center of channel.
Operating Principles of FETs

- Further increasing $V_D$ will not substantially increase $I_D$ but leads to an expansion of the depletion region.

Output Characteristics

- Holding gate voltage constant and sweeping drain voltage.

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**Source-Drain Current ($I_D$)**

**Drain Voltage ($V_D$)**

**Saturation regime**

**Linear Regime**

**Semiconductor**

**Dielectric**

**Metal (Gate)**

**Drain Voltage ($V_D$)**

**Source-Drain Current ($I_D$)**

**Gate Voltage ($V_G$)**
Transfer Characteristics

• Holding drain voltage constant and sweeping gate voltage.

Carrier Types
Polarity of Transistors

- Unlike materials, the type of transistor is determined by the relative position of conduction and valence bands relative to work function of electrodes.

“N-Type”

“P-Type”

Gate Voltage

Gate Voltage

N-Type Transistors

- N-type transistors transport electrons but not holes.
**P-Type Transistors**

- P-type transistors transport holes but not electrons.

![Diagram of P-type transistor]

**Ambipolar Transistors**

- Ambipolar (sometimes called bipolar) transistors are unique in that they can inject and transport both holes and electrons, under the correct biasing conditions.

![Diagram of ambipolar transistor]
Combining Transistors

• We can consider transistors as voltage-controlled resistors. E.g. for an n-type transistor:

  - **Negative Voltage**
    - High Resistance
    - Gate Voltage
    - Low Resistance
    - +V
  
  - **Zero Voltage**
    - High Resistance
    - Gate Voltage
    - +V
  
  - **Positive Voltage**
    - Low Resistance
    - Gate Voltage
    - +V
Combining Transistors

- We can consider the below circuit as a potential divider.

\[ V_{DD} \quad V_{in} \quad V_{out} \quad V_{DD} \quad V_{out} \]

\[ P\text{-Type} \quad N\text{-Type} \]

\[ V_{in} \quad V_{out} \quad V_{out} \]

If \( V_{DD} = 5V \), \( V_{in} = 0V \). What is \( V_{out} \)?
Combining Transistors

- Start by looking at the n-type transistor.

\[ V_{DD} \]
\[ +5V \]
\[ V_{in} \]
\[ 0V \]
\[ P-Type \]
\[ N-Type \]
\[ V_{out} \]

Combining Transistors

- Consider the transfer-curve for this FET.

\[ V_{DD} \]
\[ +5V \]
\[ V_{in} \]
\[ 0V \]
\[ P-Type \]
\[ N-Type \]
\[ V_{out} \]
\[ I_D \]
\[ 0V \]
\[ Gate Voltage \]
Combining Transistors

- If $V_{DD} = 5V$, $V_{in} = 0V$. What is $V_{out}$?

Since, under these biasing conditions the FET is off, we can consider this FET as a break.

Combining Transistors

- Now look at the p-type transistor.
Combining Transistors

• Since potentials are relative we can instead describe the FET in a more recognizable form.

\[ V_{DD} \]
\[ +5V \]
\[ V_{in} \]
\[ 0V \]
\[ +5V \]
\[ V_{out} \]
\[ N-Type \]
\[ P-Type \]

\[ P-Type \]
\[ -5V \]

Combining Transistors

• Consider the transfer-curve for this FET.

\[ V_{DD} \]
\[ +5V \]
\[ V_{in} \]
\[ 0V \]
\[ +5V \]
\[ V_{out} \]
\[ N-Type \]
\[ P-Type \]
\[ I_D \]
\[ -5V \]

Gate Voltage
Combining Transistors

• If \( V_{DD} = 5V, V_{in} = 0V \). What is \( V_{out} \)?

Under these biasing conditions, we can consider this FET as a wire.

\[
\begin{align*}
V_{DD} & = +5V \\
V_{in} & = 0V \\
V_{out} & = +5V
\end{align*}
\]

Combining Transistors

• Now, if \( V_{DD} = 5V, V_{in} = +5V \). What is \( V_{out} \)?

\[
\begin{align*}
V_{DD} & = +5V \\
V_{in} & = +5V \\
V_{out} & = +5V
\end{align*}
\]
Combining Transistors

- Start with our n-type transistor again:

- Again, consider the transfer-curve under these biases.
Combining Transistors

• Now, if $V_{DD} = 5V$, $V_{in} = +5V$. What is $V_{out}$?

  In this case our n-type FET is on, so we model it as a piece of wire.

Combining Transistors

• Finally, consider our p-type transistor again:
Combining Transistors
• Again, since the difference between source and gate are zero we can re-draw this:

\[ V_{DD} \]

\[ 0V \]

\[ V_{in} \]

\[ +5V \]

\[ V_{out} \]

\[ +5V \]

\[ N-Type \]

\[ P-Type \]


Combining Transistors
• We can now draw the p-type transfer curve:

\[ V_{DD} \]

\[ 0V \]

\[ V_{in} \]

\[ +5V \]

\[ V_{out} \]

\[ +5V \]

\[ N-Type \]

\[ P-Type \]

\[ I_D \]

\[ 0V \]

\[ Gate Voltage \]
Combining Transistors

- Now, if $V_{DD} = 5V$, $V_{in} = +5V$. What is $V_{out}$?

Now, our p-type transistor is off, so we can describe it as a break.

Combining Transistors

- Exact behavior of $V_{out}$ vs $V_{in}$ depends on properties of transistors.

Exact behavior of $V_{out}$ vs $V_{in}$ depends on properties of transistors.
Combining Transistors

- But we can identify this as an inverter. The most simple building block of a logic circuit.

\[
V_{DD} \quad P-\text{Type} \quad N-\text{Type} \quad V_{in} \quad V_{out} \quad +5V \quad 0V \quad 0V \quad +5V \quad V_{in} \quad V_{out}
\]

<table>
<thead>
<tr>
<th>(V_{in})</th>
<th>(V_{out})</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Next Time...

- FETs Characteristics.

- Quantifying FETs, and extracting parameters.

\[
I_D = \frac{W}{L} \mu C_{ox} \left( (V_G - V_T)V_D - \frac{V_D^2}{2} \right)
\]