Lecture 14: Field Effect Transistors Part II

Announcements

Laboratory Report 1/2:

- The report is due today.
- Please bring your hard copy up to me now.
- I will return your graded reports two weeks from today (Wednesday May 22\textsuperscript{nd}).
Last Time

- Before the break we looked at the basics of field effect transistors.

Lecture 14

- Threshold Voltage.
- Current-Voltage Behavior.
- Combining FETs.
Threshold Voltage

MOSFETs

- Recall, our inversion-mode MOSFET looks something like the following:

- Last time we simply stated that by applying some gate voltage we would induce inversion, and make the channel conducting.
- We did not specify what voltage we needed to apply.
Inversion

- Recall from Lecture 6, that for inversion to occur we require:
  - \( \phi_{Bp} < \phi_s \).
- Where:
  - \( \phi_{Bp} \) is the bulk potential.
  - \( \phi_s \) is the surface potential.
- Hence we see immediately that we require a certain applied voltage to reach this condition.
- However, there are other factors that affect the voltage required to turn on a transistor...

Aside: Surface Potential

- For a two-terminal MOS Capacitor the surface potential is easy to define:
- However in an MOSFET we have a 2-dimensional field:
  - So the surface potential is a function of position.
  - For high \( V_{DS} \) inversion will not occur everywhere.
  - This is why we see pinch-off.
Trapped Charge

- Not all charge will contribute to transport.
- Consider the interface by the inversion layer.
- Some injected charge will fill traps and be immobile.
- Some already-trapped charge will be released and become mobile.
- Also, the semiconductor, dielectric, and the interface may not be electrically neutral at $V_G = 0$.
- These factors all affect the threshold voltage.

Threshold Voltage

- When it comes to quantifying the charge density in the channel for a certain applied voltage, we could treat the dielectric as we did in Lecture 6:

\[
Q' = C_i V_{GS} \frac{A}{A} = C_i V_{GS}
\]

We will explain why we use a prime (') shortly.
Threshold Voltage

- When it comes to quantifying charge transport, we want to know how much mobile charge is present in the channel.
- We have just seen that to induce mobile electrons we need to first satisfy the conditions for inversion, and also account for any persistent background charge at the interface.

- The common approach is to define a threshold voltage ($V_T$), which needs to be overcome before mobile charges are induced. All effects are encapsulated in this parameter.

\[ E_{Fm} \geq E_{Fs} \geq E_V \geq E_C \geq d \geq E_i \]

Threshold Voltage

- The threshold voltage encapsulates all the behavior we have discussed, and is not necessarily a static quantity.
- UV light can also induce trapping and de-trapping in certain systems.
Threshold Voltage

- We can derive the threshold voltage from the bulk potential, flat-band voltage and a few other parameters.
- However this is beyond the scope of this course, and we will simply consider $V_T$ an empirical parameter.
- More details can be found in ECE616 or Sze and Ng Physics of Semiconductor Devices Section 6.2.
- We will just say, to induce a mobile charge density (Q/cm$^2$) of $Q_{mob}$ we require an applied $V_{GS}$ of:

$$Q_{mob} = \frac{C_i}{A} (V_{GS} - V_T)$$

- $V_T$ can be positive or negative depending on the charge density at the interface.

Current-Voltage Behavior
Current Voltage Behavior

- Ultimately, we want to be able to predict the output current of an FET, for a certain set of applied gate and drain voltages, and device parameters.
- I.e. we want to be able to predict something like the following from some simple input parameters.

![Figure 9.9: Brotherton](image)

Current Voltage Behavior

- The derivation is not that complex, but we will not be doing it today. Other classes cover it:
  - ECE613, ECE616, ECE617.
  - The transistor channel is defined to have a certain length ($L$), width ($W$) and depth ($D$):

![Diagram of transistor channel](image)

- Carriers flow left→right or right→left in this diagram.
Current Voltage Behavior

- Since the mobile charge density \( Q_{\text{mob}} \) is not uniform in the channel, the transistor channel has to be split into small sections of length \( \delta y \):

- To evaluate the current, \( \delta y \to 0 \) and an integration is carried out across the channel.
- Carrier density is then used to evaluate resistivity and then current.

- This final assumption is what is called the gradual channel approximation.
- Only drift current will be considered (diffusion current is ignored).
- Doping in the channel is uniform.
- Leakage current is negligible.
- The transverse field \( E_z \) (\perp \) to current flow) is much greater than the longitudinal field \( E_y \) (\parallel \) to current flow).
- This final assumption is what is called the gradual channel approximation.
- The solution to the derivation is sometimes called the gradual channel approximation (GCA).
Gradual Channel Approximation

- The main equation for the gradual channel approximation is:

\[ I_{DS} = \frac{W}{AL} \mu C_i \left( (V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right) \]

- Where:
  - \( I_{DS} \) is the source-drain current.
  - \( W \) is the channel width.
  - \( A \) is the device area.
  - \( \mu \) is the charge carrier mobility.
  - \( C_i \) is the oxide capacitance.
  - \( V_{GS} \) is the gate voltage.
  - \( V_{DS} \) is the drain voltage.
  - \( V_T \) is the threshold voltage.

Mobility in Research

- A large motivation for a lot of work in emerging electronics is to improve charge carrier mobility.

Labram et al. Small 11, 5472 (2015)
Mobility Extraction

- There are two main ways in which mobility is extracted from $IV$ characteristics.
  - In the linear regime $\rightarrow$ linear mobility ($\mu_{\text{lin}}$).
  - In saturation regime $\rightarrow$ saturation mobility ($\mu_{\text{sat}}$).
- Recall what output curves look like:

Linear Regime

- We consider the FET in the **linear regime** when:
  $$|V_{DS}| \ll |V_{GS} - V_T|$$
- We can use this to say:
  $$\left( V_{GS} - V_T \right)V_{DS} \gg \frac{V_{DS}^2}{2}$$
- Apply this approximation to the GCA Equation:
  $$I_{DS} = \frac{W}{AL} \mu_{\text{lin}} C_i \left( V_{GS} - V_T \right)V_{DS}$$
- $\mu_{\text{lin}}$ denotes this is **only valid in the linear regime**.
Linear Regime

\[ I_{DS} = \frac{W}{AL} \mu_{\text{lin}} C_i (V_{GS} - V_T) V_{DS} \]

- We actually tend to evaluate \( \mu \) from transfer characteristics, rather than output characteristics.
- This is because it turns out we don’t need to know \( V_T \).

Output

Transfer

\[ dI_{DS} \quad dV_{GS} \]

\[ \mu = \frac{LA}{WC_i V_{DS}} \frac{dI_{DS}}{dV_{GS}} \]
Linear Mobility

\[ \mu_{\text{lin}} = \frac{LA}{WC_iV_{DS}} \frac{dI_{DS}}{dV_{GS}} \]

- Notice, we don’t need to know \( V_T \) now.
- We just need to know the channel dimensions (length, width and area), and the dielectric capacitance.
  - These are normally very easy to determine.
- It is important to emphasize that this is only valid in the linear regime.
- Hence only if:
  \[ |V_{DS}| \ll |V_{GS} - V_T| \]

Numerical Differentiation

- You are all familiar with differentiating mathematical functions:
  \[ y(x) = x^2 \quad \Rightarrow \quad \frac{dy}{dx} = 2x \]
- But the concept of differentiating real data may be new to some of you.
- Numerical differentiation is important to FET mobility analysis.
  - And also many other techniques.
- If you have experimental data of \( I_{DS} \) vs \( V_{GS} \), how do you determine \( \frac{dI_{DS}}{dV_{GS}} \)?
Numerical Differentiation

- When going from analytical functions to real data, we have to consider derivatives as difference equations:

\[ \frac{dy}{dx} \rightarrow \frac{\Delta y}{\Delta x} \]

- Where \( \Delta y \) and \( \Delta x \) are now finite steps.
- To find the derivative at a data point \( i \) we need to consider adjacent points \( i - 1 \) and \( i + 1 \).

\[ \frac{\Delta y}{\Delta x} = \frac{y_{i+1} - y_{i-1}}{x_{i+1} - x_{i-1}} \]

Derivatives for the end points are not defined.

Linear Example Data

- Here is what some real data looks like differentiated:
Linear Mobility

- In the linear regime we can only consider data where $|V_{DS}| \ll |V_{GS} - V_T|$.
- Normally some average is taken in the correct part of the curve.
- Here:
  \[
  \frac{dI_{DS}}{dV_{GS}} \approx 1 \times 10^{-6} \text{A/V}
  \]
  \[
  \mu_{\text{lin}} = \frac{LA}{WC_iV_{DS}} \frac{dI_{DS}}{dV_{GS}}
  \]

- The rest of the parameters are known:
  - $V_{DS}$, $L$, $W$, $A$, $C_i$.

Combining FETs
Combining Transistors

- We can consider transistors as voltage-controlled resistors. E.g. for an n-type transistor:

  - **Negative Voltage**
    - High Resistance
    - Gate Voltage: -V
    - Current: I_D

  - **Zero Voltage**
    - High Resistance
    - Gate Voltage: 0V
    - Current: I_D

  - **Positive Voltage**
    - Low Resistance
    - Gate Voltage: +V
    - Current: I_D

Combining Transistors

- We can consider the below circuit as a potential divider.

  - **V_Dn**
  - **V_Dp**
  - **V_in**
  - **V_out**

  - **P-Type**
  - **N-Type**
Combining Transistors

- If $V_{DD} = 5V$, $V_{in} = 0V$. What is $V_{out}$?

Combining Transistors

- Start by looking at the n-type transistor.
Combining Transistors

• Consider the transfer-curve for this FET.

\[ V_{DD} \]

\[ V_{in} \]

\[ V_{out} \]

P-Type

N-Type

\[ 0V \]

\[ +5V \]

\[ +5V \]

\[ 0V \]

\[ I_D \]

\[ 0V \]

Gate Voltage

Combining Transistors

• If \( V_{DD} = 5V, V_{in} = 0V \). What is \( V_{out} \)?

Since, under these biasing conditions the FET is off, we can consider this FET as a break.
Combining Transistors
• Now look at the p-type transistor.

Combining Transistors
• Since potentials are relative we can instead describe the FET in a more recognizable form.
Combining Transistors

• Consider the transfer-curve for this FET.

\[ V_{DD} \]
\[ +5V \]
\[ V_{in} \]
\[ 0V \]
\[ +5V \]
\[ V_{out} \]

\[ -5V \]

Gate Voltage

\[ I_D \]

\[ V_{DD} \]
\[ +5V \]
\[ V_{in} \]
\[ 0V \]
\[ +5V \]
\[ V_{out} \]

P-Type

N-Type

Combining Transistors

• If \( V_{DD} = 5V, V_{in} = 0V \). What is \( V_{out} \)?

Under these biasing conditions, we can consider this FET as a wire.

\[ V_{DD} \]
\[ +5V \]
\[ V_{in} \]
\[ 0V \]
\[ +5V \]
\[ V_{out} \]

P-Type

N-Type

\[ V_{out} \]

\[ +5V \]

\[ 0V \]

\[ V_{in} \]
Combining Transistors

• Now, if $V_{DD} = 5V$, $V_{in} = +5V$. What is $V_{out}$?

Combining Transistors

• Start with our n-type transistor again:
Combining Transistors

• Again, consider the transfer-curve under these biases.

\[ V_{DD}, 0V, V_{in}, +5V, V_{out} \]

\[ P-Type \]

\[ N-Type \]

\[ I_D \]

\[ +5V \]

\[ Gate Voltage \]

\[ V_{DD} \]

\[ 0V \]

\[ V_{in} \]

\[ +5V \]

\[ V_{out} \]

\[ +5V \]

\[ 0V \]

\[ V_{in} \]

\[ V_{out} \]

In this case our n-type FET is on, so we model it as a piece of wire.
Combining Transistors

• Finally, consider our p-type transistor again:

\[ V_{DD} \]
\[ 0V \]
\[ V_{in} \]
\[ +5V \]
\[ +5V \]
\[ V_{out} \]
\[ P-Type \]
\[ N-Type \]
\[ +5V \]
\[ +5V \]
\[ 0V < V_{out} < 5V \]

Combining Transistors

• Again, since the difference between source and gate are zero we can re-draw this:

\[ V_{DD} \]
\[ 0V \]
\[ V_{in} \]
\[ +5V \]
\[ +5V \]
\[ V_{out} \]
\[ P-Type \]
\[ N-Type \]
\[ +5V \]
\[ -5V < V < 0V \]
Combining Transistors

- We can now draw the p-type transfer curve:

Now, if $V_{DD} = 5V$, $V_{in} = +5V$. What is $V_{out}$?

Now, our p-type transistor is off, so we can describe it as a break.
Combining Transistors

• Exact behavior of $V_{out}$ vs $V_{in}$ depends on properties of transistors.

Combining Transistors

• But we can identify this as an inverter. The most simple building block of a logic circuit.
Other Logic Gates

- The same process can be applied to other logic gates.

NAND

- NOR

Summary

- We looked at the basics of quantifying field effect transistors (current vs voltage).

\[ I_{DS} = \frac{W}{AL} \mu C_i \left[ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] \]

- We also looked at what happens when we combine transistors.
Next Time...

- We will cover the basics of modelling using Athena & Atlas.