1. NMOS Fabrication flow (contd.)

In the previous session, we have fabricated the NMOSFET until diffusion etch mask, which comprises of the layers shown in Fig 1.

Fig 1. (a) Diffusion window etch mask (b) Final pattern after spin-on diffusion step (c) Cross-section of transistor layers after spin-on diffusion step.

Now, we move on to finishing up the fabrication of a planar NMOSFET using the following steps.

(i) Patterning gate oxide window
(ii) Growing a 70 nm thick dry gate oxide
(iii) Patterning, Source/Drain and gate contact windows
(iv) Thermally evaporating aluminum
(v) Patterning final Aluminum contacts
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2. Gate Window mask

Now that we’ve created source and drain n-wells in a p-type silicon substrate, we can now move on to patterning a window to grow a gate oxide, that can be used to create MOS-capacitor like structure to turn our NMOS transistor ON or OFF.

We perform lithography on our patterned substrate with a second mask layer – A Gate window etch mask (a dark field mask), shown in Fig 2.

![Fig 2. (a) Diffusion window etch mask (b)Final pattern after spin-on diffusion step (c) Cross-section of transistor layers after spin-on diffusion step.](image)

2a. Mask Alignment

To pattern our second mask layer, we need to align this pattern with the existing pattern on our substrate using the help of “E” like alignment marks present on both our substrate and the second mask. The following video demonstrates how to perform alignment using a Karl Suss MA6 mask aligner.
Fig 3. 4 simple steps to align a pre-patterned substrate to a fixed light field mask.

1. Adjust rotational mis-alignment by $\Theta_{\text{error}}$.

2. Correct translational mis-alignment by $x_{\text{error}}$ and $y_{\text{error}}$.

3. Check for mis-alignment on a higher magnification.

4. Repeat same procedure if mis-aligned on a finer scale until perfectly aligned.
The following tips should be helpful when aligning a mask with a pre-patterned substrate.

1. Make sure the substrate is just out of contact with the mask (with a few microns spacing between the mask and the substrate), also known as “SEPERATION” to perform your alignment procedure.
2. Start off by performing a rotational alignment followed by translational alignment.
3. Make sure to place your aligned substrate in “CONTACT” with the mask before exposure.

- After exposure, develop your patterned substrate for 1 min MF-321 developer followed by a D.I. water wash.
- You can then etch the patterned gate oxide window in BOE etch followed by a photoresist strip as shown in Fig 2.
- The etch time can be calculated from the total oxide thickness to be etched, which is P-glass thickness (~150 nm) + Field oxide thickness (~600 nm).

**2b. Gate oxide growth**

Once the gate oxide window has been formed, we can grow a 70 nm gate oxide using dry oxidation as shown in Fig 4.

![Gate window etch](image)

**Gate window etch**

F OX → **Field oxide (Wet SiO₂)**

G OX → **Gate oxide (dry SiO₂)**

- n-well
- Phosphorous glass (basically SiO₂ with some P dopant)

![Gate oxide growth](image)

**Gate oxide growth**

Dry oxidation is a common process used to grow a thin, high quality SiO₂ gate oxide. A dry oxide, grown in an oxidation furnace using O₂ is usually of better quality compared to a wet oxide, using steam. Expected dry oxide thickness can be calculated using the deal grove model, shown in equation (1).
Where $t \rightarrow$ time required to grow oxide [in hours]
x$_0$ $\rightarrow$ Final oxide thickness (to be solved for) [in µm]
x$_i$ $\rightarrow$ initial oxide thickness [in µm]

B and B/A are rate constants that depend on (i) temperature (ii) pressure and (iii) crystal orientation of the wafer. These parameters can be calculated for given process conditions using equations (2) and (3) and values from table 1, for a silicon wafer of crystal orientation <111>. B/A is the only rate constant that changes between a <100> and <111> wafer, given by the relation in equation (4).

<table>
<thead>
<tr>
<th></th>
<th>B</th>
<th>B/A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dry O₂</td>
<td>$C_1 = 7.72 \times 10^7$ µm$^2$/hr</td>
<td>$C_2 = 6.23 \times 10^6$ µm/hr</td>
</tr>
<tr>
<td></td>
<td>$E_1 = 1.23$ eV</td>
<td>$E_2 = 2.00$ eV</td>
</tr>
</tbody>
</table>

\[
B = C_1 \exp \left( - \frac{E_1}{kT} \right) \quad (2)
\]
\[
\frac{B}{A} = C_2 \exp \left( - \frac{E_2}{kT} \right) \quad (3)
\]
\[
\frac{B}{A(111)} = 1.68 \cdot \frac{B}{A(100)} \quad (4)
\]

Table 1. Rate constants for a <111> silicon wafer

Where $k$ is the Boltzmann’s constant (in eV/K) and $T$ is the process temperature (in K).

Once a 70 nm gate oxide is grown (can be measured using ellipsometry), it is time to etch Aluminum contact windows for metallization.

### 3. Contact Window mask & Etch

In this step we protect the gate oxide grown in the previous step and etch through the oxide layers present on the source and drain n-well regions to make Al contacts in the subsequent step. This again follow a lithography $\rightarrow$ etch process shown in Fig 5.

The total oxide thickness that needs to be etched is **Gate oxide + Field oxide + P-glass thickness.**
4. Aluminum contact mask

The final mask involves patterning thermally evaporated aluminum (~100 nm) to make contacts for measuring the electrical characteristics of NMOS transistors and other devices present on the wafer. Fig 6 shows a dep-photo-etch loop to make the final transistor structure.

A **hard bake (150C, 5 min on a hot-plate)** is done after UV exposure and pattern development to protect the photoresist from an aggressive oxidizing etch due to Aluminum type A etchant (a mixture of 80% Phosphoric acid: 5% Nitric acid: 5% acetic acid: remaining H2O). The following video shows a blanket etch of aluminum deposited on a silicon wafer. You can see that:
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(i) Aluminum etchant has a higher etch rate and this rate increases with increase in temperature.

(ii) It is hard to calculate the exact etch time (and hence it may not be a great measure to detect end-point) since
   a. Al type A etchant has a high etch rate, even at room temperature.
   b. The etch time varies based on when the acid breaks through the thin oxide layer of Al₂O₃ in a certain part of the wafer. This causes different parts of the wafer to etch at different rates.

(ii) The end-point is clearly visible (the wafer loses its shiny metallic luster from aluminum at the etch endpoint).

PPE required: Nitrile gloves, face shield, Splash protection suit.

Post-etch, the wafer is thoroughly rinsed with D.I. water and the photoresist stripped by a thorough AID clean. The final processed structure should resemble the optical image shown in Fig 7. Your transistors are now ready for electrical measurement.

Fig 7. Final die structure after Aluminum etch patterning