Last Time

• Before the break we looked at the basics of field effect transistors.
Lecture 14

• Threshold Voltage.
• Current-Voltage Behavior.
• Combining FETs.

Threshold Voltage
MOSFETs

- Recall, our inversion-mode MOSFET looks something like the following:

  ![MOSFET diagram]

- Last time we simply stated that by applying some gate voltage we would induce inversion, and make the channel conducting.
- We did not specify what voltage we needed to apply.

Inversion

- Recall from Lecture 8, that for inversion to occur we require:
  - $\phi_{BP} < \phi_S$.
- Where:
  - $\phi_{BP}$ is the bulk potential.
  - $\phi_S$ is the surface potential.
- Hence we see immediately that we require a certain applied voltage to reach this condition.
- However, there are other factors that affect the voltage required to turn on a transistor...
Aside: Surface Potential

- For a two-terminal MOS Capacitor the surface potential is easy to define:
- However in an MOSFET we have a 2-dimensional field:

\[ E_F \]

- So the surface potential is a function of position.
- For high \( V_{DS} \) inversion will not occur everywhere.
- This is why we see pinch-off.

Trapped Charge

- Not all charge will be contribute to transport.
- Consider the interface by the inversion layer.

- Some injected charge will fill traps and be immobile.
- Some already-trapped charge will be released and become mobile.

- Also, the semiconductor, dielectric, and the interface may be not be electrically neutral at \( V_G = 0 \).
- These factors all affect the threshold voltage.
Threshold Voltage

- When it comes to quantifying the charge density in the channel for a certain applied voltage, we could treat the dielectric as we did in Lecture 8:

\[ V > 0 \]

- For a gate oxide with capacitance of \( C_i \) we could say the total charge/area was:

\[ Q' = \frac{C_i V_{GS}}{A} \]

\( A = \) device area

We will explain why we use a prime (') shortly

We have just seen that to induce mobile electrons we need to first satisfy the conditions for inversion, and also account for any persistent background charge at the interface.

- The common approach is to define a threshold voltage (\( V_T \)), which needs to be overcome before mobile charges are induced. All effects are encapsulated in this parameter.

Threshold Voltage

- When it comes to quantifying charge transport, we want to know how much mobile charge is present in the channel.

- We have just seen that to induce mobile electrons we need to first satisfy the conditions for inversion, and also account for any persistent background charge at the interface.
Threshold Voltage

- The threshold voltage encapsulates all the behavior we have discussed, and is not necessarily a static quantity.
- UV light can also induce trapping and de-trapping in certain systems.

We can derive the threshold voltage from the bulk potential, flat-band voltage and a few other parameters.

However this is beyond the scope of this course, and we will simply consider $V_T$ an empirical parameter.

More details can be found in ECE616 or Sze and Ng Physics of Semiconductor Devices Section 6.2.

We will just say, to induce a mobile charge density (Q/cm$^2$) of $Q_{mob}$ we require an applied $V_{GS}$ of:

$$Q_{mob} = \frac{C_i}{A} (V_{GS} - V_T)$$

$V_T$ can be positive or negative depending on the charge density at the interface.
Current-Voltage Behavior

- Ultimately, we want to be able predict the output current of an FET, for a certain set of applied gate and drain voltages, and device parameters.
- I.e. we want to be able to predict something like the following from some simple input parameters.

Fig 9.9. Brotherton
Current Voltage Behavior

- The derivation is not that complex, but we will not be doing it today. Other classes cover it:
  - ECE613, ECE616, ECE617.
- The transistor channel is defined to have a certain length ($L$), width ($W$) and depth ($D$):

  ![Diagram of transistor channel]

- Carriers flow left→right or right→left in this diagram.

Current Voltage Behavior

- Since the mobile charge density ($Q_{mob}$) is not uniform in the channel, the transistor channel has to be split into small sections of length $\delta y$:

  ![Diagram showing channel splitting]

- To evaluate the current, $\delta y \to 0$ and an integration is carried out across the channel.
- Carrier density is then used to evaluate resistivity and then current.
Current Voltage Behavior

- The assumptions made in the derivation are:
  - Only drift current will be considered (diffusion current is ignored).
  - Doping in the channel is uniform.
  - Leakage current is negligible.
  - The transverse field $E_z$ ($\perp$ to current flow) is much greater than the longitudinal field $E_y$ ($\parallel$ to current flow).
  - This final assumption is what is called the gradual channel approximation.
  - The solution to the derivation is sometimes called the gradual channel approximation (GCA).

Gradual Channel Approximation

- The main equation for the gradual channel approximation is:

$$I_{DS} = \frac{W}{AL} \mu C_i \left[ (V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right]$$

- Where:
  - $I_{DS}$ is the source-drain current.
  - $W$ is the channel width.
  - $L$ is the channel length.
  - $A$ is the device area.
  - $\mu$ is the charge carrier mobility.
  - $C_i$ is the oxide capacitance.
  - $V_{GS}$ is the gate voltage.
  - $V_{DS}$ is the drain voltage.
  - $V_T$ is the threshold voltage.
Mobility in Research

- A large motivation for a lot of work in emerging electronics is to improve charge carrier mobility.

Labram et al. Small 11, 5472 (2015)

Mobility Extraction

- There are two main ways in which mobility is extracted from $IV$ characteristics.
  - In the linear regime $\rightarrow$ linear mobility ($\mu_{\text{lin}}$).
  - In saturation regime $\rightarrow$ saturation mobility ($\mu_{\text{sat}}$).
- Recall what output curves look like:
Linear Regime

- We consider the FET in the **linear regime** when:
  \[ |V_{DS}| \ll |V_{GS} - V_T| \]

- We can use this to say:
  \[ (V_{GS} - V_T)V_{DS} \gg \frac{V_{DS}^2}{2} \]

- Apply this approximation to the GCA Equation:
  \[ I_{DS} = \frac{W}{AL} \mu_{lin} C_i (V_{GS} - V_T)V_{DS} \]

- \( \mu_{lin} \) denotes this is **only valid in the linear regime**.

---

Linear Regime

\[ I_{DS} = \frac{W}{AL} \mu_{lin} C_i (V_{GS} - V_T)V_{DS} \]

- We actually tend to evaluate \( \mu \) from **transfer characteristics**, rather than output characteristics.

- This is because it turns out we don’t need to know \( V_T \).
Linear Regime

- The way this is usual done is by **numerically differentiating** the transfer curve.
- Recall that the transfer curve is $I_D$ plotted against $V_G$:

  $$I_{DS} = \frac{W}{AL} \mu_{lin} C_i (V_{GS} - V_T) V_{DS}$$

  $$\frac{dI_{DS}}{dV_{GS}} = \frac{W}{AL} \mu_{lin} C_i V_{DS} \quad \mu_{lin} = \frac{LA}{WC_i V_{DS}} \frac{dI_{DS}}{dV_{GS}}$$

Linear Mobility

- Notice, we don’t need to know $V_T$ now.
- We just need to know the channel dimensions (length, width and area), and the dielectric capacitance.
  - These are normally very easy to determine.
- It is important to emphasize that this is **only valid in the linear regime**.
- Hence only if:

  $$|V_{DS}| \ll |V_{GS} - V_T|$$
Numerical Differentiation

- You are all familiar with differentiating mathematical functions:
  \[ y(x) = x^2 \]
  \[ \frac{dy}{dx} = 2x \]

- But the concept of differentiating real data may be new to some of you.
- Numerical differentiation is important to FET mobility analysis.
  - And also many other techniques.
- If you have experimental data of \( I_{DS} \) vs \( V_{GS} \), how do you determine \( \frac{dI_{DS}}{dV_{GS}} \)?

When going from analytical functions to real data, we have to consider derivatives as difference equations:

\[ \frac{dy}{dx} \approx \frac{\Delta y}{\Delta x} \]

- Where \( \Delta y \) and \( \Delta x \) are now finite steps.
- To find the derivative at a data point \( i \) we need to consider adjacent points \( i - 1 \) and \( i + 1 \).

\[ \frac{\Delta y}{\Delta x} = \frac{y_{i+1} - y_{i-1}}{x_{i+1} - x_{i-1}} \]
Linear Example Data

- Here is what some real data looks like differentiated:

```
-20 0 20 40 60 80 10
-12
10
-11
10
-10
10
-9
10
-8
10
-7
10
-6
10
-5
```

\[ I_D (A) \]

\[ V_{DS} = 10V \]

```
-20 0 20 40 60 80 10
-12
10
-11
10
-10
10
-9
10
-8
10
-7
10
-6
10
\]

\[ dI_D/dV_G (A/V) \]

\[ V_{DS} = 10V \]

```

Linear Mobility

- In the linear regime we can only consider data where |V_{DS}| \ll |V_{GS} - V_T|.
- Normally some average is taken in the correct part of the curve.
- Here:

\[
\frac{dI_{DS}}{dV_{GS}} \approx 1 \times 10^{-6} A/V
\]

\[
\mu_{lin} = \frac{LA}{WC_iV_{DS}} \frac{dI_{DS}}{dV_{GS}}
\]
Combining FETs

Combining Transistors

• We can consider transistors as voltage-controlled resistors. E.g. for an n-type transistor:

  - **Negative Voltage**
    - High Resistance
    - Zero Voltage High Resistance
    - Positive Voltage Low Resistance

  ![Gate Voltage](image)
Combining Transistors

- We can consider the below circuit as a potential divider.

\[ V_{DD} \quad V_{out} \]

\[ +5V \quad 0V \]

- If \( V_{DD} = 5V, V_{in} = 0V \). What is \( V_{out} \)?
Combining Transistors

- Start by looking at the n-type transistor.

![Combining Transistors Diagram](image)

Combining Transistors

- Consider the transfer-curve for this FET.

![Combining Transistors Diagram](image)
Combining Transistors

- If $V_{DD} = 5V$, $V_{in} = 0V$. What is $V_{out}$?

Since, under these biasing conditions the FET is off, we can consider this FET as a break.

Combining Transistors

- Now look at the p-type transistor.

$0V < V_{out} < 5V$
Combining Transistors

- Since potentials are relative we can instead describe the FET in a more recognizable form.

\[ V_{DD} \]
\[ V_{in} \]
\[ 0\text{V} \]
\[ +5\text{V} \]
\[ V_{out} \]

\[ +5\text{V} \]
\[ -5\text{V} \]
\[ -5<V<0\text{V} \]

Combining Transistors

- Consider the transfer-curve for this FET.
Combining Transistors

• If $V_{DD} = 5V$, $V_{in} = 0V$. What is $V_{out}$?

Under these biasing conditions, we can consider this FET as a wire.

Combining Transistors

• Now, if $V_{DD} = 5V$, $V_{in} = +5V$. What is $V_{out}$?
Combining Transistors

• Start with our n-type transistor again:

\[ V_{DD} \]

\[ 0V \]

\[ V_{in} \]

\[ +5V \]

\[ V_{out} \]

\[ +5V \]

\[ P-Type \]

\[ 0V < V_{out} < 5V \]

\[ N-Type \]

\[ +5V \]

Combining Transistors

• Again, consider the transfer-curve under these biases.

\[ V_{DD} \]

\[ 0V \]

\[ V_{in} \]

\[ +5V \]

\[ V_{out} \]

\[ +5V \]

\[ P-Type \]

\[ I_D \]

\[ Gate Voltage \]
Combining Transistors

• Now, if $V_{DD} = 5V$, $V_{in} = +5V$. What is $V_{out}$?

$V_{DD}$

$V_{in}$

$V_{out}$

In this case our n-type FET is on, so we model it as a piece of wire.

Combining Transistors

• Finally, consider our p-type transistor again:

$V_{DD}$

$V_{in}$

$V_{out}$

$0V < V_{out} < 5V$
Combining Transistors

• Again, since the difference between source and gate are zero we can re-draw this:

\[ V_{DD} \]
\[ 0V \]
\[ V_{in} \]
\[ +5V \]
\[ V_{out} \]
\[ +5V \]
\[ N-Type \]
\[ -5V < V < 0V \]

Combining Transistors

• We can now draw the p-type transfer curve:

\[ V_{DD} \]
\[ 0V \]
\[ V_{in} \]
\[ +5V \]
\[ V_{out} \]
\[ +5V \]
\[ N-Type \]
Combining Transistors

- Now, if $V_{DD} = 5V$, $V_{in} = +5V$. What is $V_{out}$?

Now, our p-type transistor is off, so we can describe it as a break.

Combining Transistors

- Exact behavior of $V_{out}$ vs $V_{in}$ depends on properties of transistors.
Combining Transistors

- But we can identify this as an inverter. The most simple building block of a logic circuit.

\[ V_{DD} \]
\[ V_{in} \]
\[ V_{out} \]

- P-Type

\[ V_{out} \]
\[ +5V \]

- N-Type

\[ 0V \]
\[ 0V \]
\[ +5V \]

\[ V_{in} \]

<table>
<thead>
<tr>
<th>( V_{in} )</th>
<th>( V_{out} )</th>
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<tbody>
<tr>
<td>0</td>
<td>1</td>
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<tr>
<td>1</td>
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Other Logic Gates

- The same process can be applied to other logic gates.

NAND

\[ A \quad B \quad \rightarrow \quad \text{out} \]

NOR

\[ A \quad B \quad \rightarrow \quad \text{out} \]
Summary

- We looked at the basics of quantifying field effect transistors (current vs voltage).

\[ I_{DS} = \frac{W}{AL} \mu_C \left[ (V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right] \]

- We also looked at what happens when we combine transistors.

\[ \begin{array}{c|c}
V_{in} & V_{out} \\
0 & 1 \\
1 & 0 \\
\end{array} \]

Next Time...

- We will talk about ion implantation.