Switched-Capacitor Track-and-Hold Amplifier with Low Sensitivity to Op-Amp Imperfections

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Outline

1. Introduction
2. Offset-Compensated SC Amps
3. Proposed T/H Amplifier with Gain-and Offset-Compensation
4. Simulation Results
5. Conclusions
1. Introduction
Introduction

Sample-and-hold (S/H) stage

Track-and-hold (T/H) stage

with well-controlled gain

Applications:
- data converters
- signal processing systems
Introduction

Such amplifier stages should be insensitive to the imperfections of the op-amps used.
Op-Amp Imperfections

1. finite gain
2. limited slew rate and bandwidth
3. offset and noise
4. nonlinearity
In this Presentation

A novel T/H amplifier stage is proposed to realize an accurate gain with low sensitivity to finite op-amp gain and offset voltage.
Importance of Gain Compensation

It was reported that an SC circuit with a small gain error reduced harmonic distortion caused by op-amp nonlinearity.

Huang, P.F. Ferguson, and G.C. Temes,
2. Offset-Compensated SC Amplifiers
Offset-Compensated SC Amplifiers

General structure

$\phi_1$: (input) sampling phase

$\phi_2$: (output) valid phase
Offset-Compensated SC Amplifiers

\[ v_{out}(t) = \frac{C_1}{C_2} v_{in}\left(n - \frac{1}{2}\right) + \left(1 + \frac{C_1}{C_2}\right) \left[v_x(t) - v_x\left(n - \frac{1}{2}\right)\right]. \]

Ideal response

Error
Offset-Compensated SC Amplifiers

\[ V_x(t) = V_{os} - \frac{V_{out}(t)}{A} \]

- \( A \): dc gain of the op-amp
- \( V_{os} \): offset voltage
Correlated Double Sampling

\[ \Delta V_x = V_x(t) - V_x(n - 1/2) \]
\[ = - \frac{\Delta V_{out}}{A} \]

where

\[ \Delta V_{out} = V_{out}(t) - V_{out}(n - 1/2) \]

If \( A \) is large, \( \Delta V_x \) is negligible.
Correlated Double Sampling

\[ v_{out}(t) = \frac{C_1}{C_2} v_{in}(n - \frac{1}{2}) + \left(1 + \frac{C_1}{C_2}\right) \Delta v_x \]

\[ \Delta V_x = - \Delta V_{out} / A \quad \text{Error} \]

If \( A \) is not large enough, \( \Delta V_{out} \) should be as small as possible for reducing the error term.
3. Proposed T/H Amplifier with Gain- and Offset-Compensation
Proposed T/H SC Amplifier

\[ \frac{v_{out}}{v_{in}} = \frac{C_1}{C_2} \]

signal path

CDS path for tracking mode

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During $\phi_1 = 1$

\[ v_{out}(t) = \frac{C_1}{C_2} v_{in}(t) + \left(1 + \frac{C_1}{C_2}\right) v_x(t) \]
During $\phi_2 = 1$

\[
v_{out}(t) = \frac{C_1}{C_2} v_{in} \left( n - \frac{1}{2} \right) + \left( 1 + \frac{C_1}{C_2} \right) \Delta v_x
\]
\[ \Delta V_{out} = V_{out}(n) - V_{out}(n - 1/2): \text{ very small} \]

\[ \frac{C_1}{C_2} v_{in}(n - \frac{1}{2}) + (1 + \frac{C_1}{C_2}) v_x(n - \frac{1}{2}) \]

\[ \frac{C_1}{C_2} v_{in}(n - \frac{1}{2}) + \left(1 + \frac{C_1}{C_2}\right) \Delta v_x \]

tracking period

holding period

\[ \phi_1 = 1 \]

\[ \phi_2 = 1 \]

\[ t / T \]
Important Point

The output at the end of the tracking period is very close to the output during the holding period.

ΔVout is negligible even for high frequency input signal.

The gain error is reduced in a wide frequency range.
Transfer Function

\[ H = \frac{C_1}{C_2} \left\{ 1 - \left( 1 + \frac{C_1}{C_2} \right) / A^2 \right\} = \frac{C_1}{C_2} (1 - E). \]

Error term \[ E = \left( 1 + \frac{C_1}{C_2} \right) / A^2 \]

Gain squaring \[ A^2 \]
# Gain Errors of SC Amplifiers

<table>
<thead>
<tr>
<th>SC amplifier</th>
<th>Error term for DC input</th>
<th>Error term for signal frequency = clock frequency/4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gregorian, 1981</td>
<td>( \left(1 + \frac{C_1}{C_2}\right)/A )</td>
<td>( \left(1 + \frac{C_1}{C_2}\right)/A )</td>
</tr>
<tr>
<td>Fujimoto, 2004</td>
<td>( \left(1 + \frac{C_1}{C_2}\right)/A )</td>
<td>( \left(1 + \frac{C_1}{C_2}\right)/A )</td>
</tr>
<tr>
<td>Haug, 1984</td>
<td>( \left(1 + \frac{C_1}{C_2}\right)^2/A^2 )</td>
<td>( \left(1 + \frac{C_1}{C_2}\right)^2/A^2 )</td>
</tr>
<tr>
<td>Larson, 1987</td>
<td>( \left(1 + \frac{C_1}{C_2}\right)^2/A^2 )</td>
<td>( \left(1 + \frac{C_1}{C_2}\right)^2/A^2 )</td>
</tr>
<tr>
<td>Yoshizawa, 1997</td>
<td>( \left(1 + \frac{C_1}{C_2}\right)^2/A^2 )</td>
<td>( \left(1 + \frac{C_1}{C_2}\right)^2/A^2 )</td>
</tr>
<tr>
<td>Proposed circuit</td>
<td>( \left(1 + \frac{C_1}{C_2}\right)^2/A^2 )</td>
<td>( \left(1 + \frac{C_1}{C_2}\right)^2/A^2 )</td>
</tr>
</tbody>
</table>

\( C_{1n} = 2C_1, C_{2n} = C_2 \)
Drawback

- A drawback of the proposed amplifier is that it requires additional capacitors.

- However, it eases the requirements on the op-amp's gain and bandwidth.

- The complexity and power dissipation of the amplifier are reduced.
4. Simulation Results
SPICE Simulation

All SC amplifiers were simulated on the transistor level in a fully differential implementation.

Gain of SC amplifier: 10
SPICE parameters: 1.2 μm CMOS process
Fully differential single-stage op-amp

DC gain = 46 dB, GBW = 2.4 MHz
For Low-Frequency Input

Signal frequency: 1.0 kHz;
Clock frequency: 31.2 kHz
For High-Frequency Input

Signal frequency: 10 kHz;
Clock frequency: 31.2 kHz
Comparison of Gain Errors by HSPICE simulations

(i) Gregorian, 1981
(ii) Haug, et al, 1984
(iv) Yoshizawa, et al, 1997
(v) Proposed circuit with $C_{1n}=2C_1$ and $C_{2n}=C_2$
# Linearity of SC Amplifiers

<table>
<thead>
<tr>
<th>SC amplifier</th>
<th>Total harmonic distortion</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$f_{in}=180$ Hz</td>
</tr>
<tr>
<td>Gregorian, 1981 (Gain-uncompensated)</td>
<td>$-58$ dB</td>
</tr>
<tr>
<td>Haug, et al, 1984 (Narrowband-compensated)</td>
<td>$-77$ dB</td>
</tr>
<tr>
<td>Larson, et al, 1987 (Wideband-compensated)</td>
<td>$-70$ dB</td>
</tr>
<tr>
<td>Proposed circuit ($C_{1n}=2C_1$, $C_{2n}=C_2$)</td>
<td>$-85$ dB</td>
</tr>
</tbody>
</table>
5. Conclusions

- Without a S/H input stage, low gain error is realized over a wide frequency range.

- Since the requirements for op-amp gain and bandwidth are alleviated, this circuit can be realized with low power consumption.

- Low harmonic distortion is expected because of offset- and gain-compensation.
RECONSTRUCTION FILTER ARCHITECTURES

a) $H_1$: biquad 1

b) $H_i$: biquad $i$

c) $H_2$: biquad 2
POST-FILTER EXAMPLES (1)

A 4\textsuperscript{th}-order Bessel filter implemented with a cascade of biquads.

Noise gains from each op-amp input

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POST-FILTER EXAMPLES (2)

A 4\textsuperscript{th}-order Bessel filter implemented with the inverse follow-the-leader topology.

Noise gains from each op-amp input