Lecture 14: MOS Capacitors – CV Plots and Non-Idealities
Sze And Ng: Chapter 4

Announcements

Homework 4/4:
• Online Tuesday 5th March.
• Due Tuesday 12th March at the start of the lecture (08:30am).
• I will return it on the day of the final (18th March).
• I will post the solutions when I return your homeworks.
• Homework 4 will consist of content covered in Lectures 12–15.

Final Exam
• The Final Examination is scheduled for Thursday 18th March 2019 at 09:30am.
• Will be in Strand Agriculture Hall 211.
• More details to follow.
Last Time

- We quantified the electric field and the electric charge density:

![Diagram showing metal, oxide, and p-type regions with electric field lines and charge densities](image)

- We then evaluated the capacitance

![Capacitance schematic with AC and DC voltages](image)

Lecture 14

- Capacitance-Voltage Plots.
- Flatband Voltage.
- Insulator Charge.
- Bias-Temperature Stressing.
Extra Information

- The below document from Harvard has a good description of accumulation, depletion, and inversion.
- Covers an n-type semiconductor rather than p-type.

Capacitance-Voltage Plots
Charge Density

• Last time we derived equations for the charge density in our MOS capacitors:

\[ Q_{sc} = \pm \frac{\sqrt{2\varepsilon_{r}\varepsilon_{0}k_{B}T}}{eL_{D}}F\left(\frac{e\phi_{s}}{k_{B}T},\frac{n_{p0}}{p_{p0}}\right) \]  

(1)

• Where:

\[ F\left(\frac{e\phi}{k_{B}T},\frac{n_{p0}}{p_{p0}}\right) = \left[\left(\exp\left(\frac{e\phi}{k_{B}T}\right) + \frac{e\phi}{k_{B}T} - 1\right) + \frac{n_{p0}}{p_{p0}}\left(\exp\left(\frac{e\phi}{k_{B}T}\right) - \frac{e\phi}{k_{B}T} - 1\right)\right]^{1/2} \]  

(2)

\[ L_{D} = \sqrt{\frac{k_{B}T\varepsilon_{r}\varepsilon_{0}}{p_{p0}e^{2}}} \]  

(3)

• Symbols are all listed in Lecture 13.

Charge Density

• We also evaluated the behavior under different operating regimes:

![Graph showing charge density behavior under different regimes](image-url)
Capacitance

- We evaluated the capacitance across the depletion region to be:

\[
C_D = \frac{dQ_{sc}}{d\phi_s} = \frac{\varepsilon_r\varepsilon_0}{\sqrt{2L_D}} \left( 1 - \exp \left( -\frac{e\phi_s}{k_B T} \right) + \frac{n_{p0}}{p_{p0}} \left( \exp \left( \frac{e\phi_s}{k_B T} \right) - 1 \right) \right)
\]  

(4)

- We describe the total capacitance \(C\) across the capacitor as two capacitors in series.

\[
\frac{1}{C} = \frac{1}{C_i} + \frac{1}{C_D}
\]  

(5)

Capacitance-Voltage Plots

- So how do we expect capacitance to change as a function of applied voltage?

- I.e. how do we populate this graph?
Accumulation

- Let’s start with a **negative** applied bias.
- Recall, from Lecture 12 that, positive and negative bias refer to the **polarity of the metal gate electrode**.

We showed in Lecture 12 that this leads to accumulation.

What does this mean for capacitance?

So here we just have a field across the dielectric, so we can say the total capacitance is just the capacitance of the insulator / oxide:

\[ C_{\text{acc}} = C_i \]
Capacitance-Voltage Plot

- On our graph we can hence draw something like the following:

\[ C = C_i \]

\[ V = 0 \]

Accumulation

---

Depletion

- What about a small positive applied bias.
- Recall, from Lecture 12 that, positive and negative bias refer to the polarity of the metal gate electrode.

- We showed in Lecture 12 that this leads to depletion.
Depletion

- What does depletion mean for capacitance?

\[ e \phi_E \quad E_i \quad E_F \quad e \phi_V \]

\[ d \]

- So once again we get a field across the insulator, but this time between holes and ionized dopant ions.
- The ionized dopant atoms are immobile and penetrate deep into the semiconductor.

### Capacitance-Voltage Plot

- The total capacitance is then given by equation (5):

\[ \frac{1}{C_{\text{depl}}} = \frac{1}{C_i} + \frac{1}{C_D} \quad (5) \]

\[ C_{\text{depl}} = \frac{C_D C_i}{C_i + C_D} \quad (6) \]

- If \( C_D \) is finite, the \( C_{\text{depl}} < C_{\text{acc}} \).
Inversion

Finally, what happens with inversion?

So in this case we have electrons at the interface, so at first glance we appear to return to just the oxide / insulator $C_i$.

However, it turns out to not be this simple...

Frequency-Dependence

For inversion to occur we require two physical processes to take place:

1). Minority carriers (holes in our case) must be repelled away from the interface, leaving ionized dopant atoms.

2). Minority carriers (electrons) in our case must be thermally generated due to Fermi-Dirac / Boltzmann statistics.
Frequency-Dependence

- The important point is that these processes occur over very different time scales.
- The movement of carriers (screening) occurs on the order of the dielectric relaxation time:
  \[ \tau_{DR} = \rho \varepsilon_0 \varepsilon_r \]  
  (7)
- Where:
  - \( \tau_{DR} \): Dielectric relaxation screening time.
  - \( \rho \): Resistivity of semiconductor.
  - \( \varepsilon_0 \varepsilon_r \): Relative permittivity of semiconductor.
  - The speed carriers move is encapsulated in \( \rho \).

Frequency-Dependence

- The generation of minority carriers occurs due to the law of mass action:
  \[ n_p p_0 = n_i^2 \]  
  (8)
- We can use this because we are in quasi-equilibrium (~no current flow).
- Technically the law of mass action is for chemical reactions.
- You can think of donors / acceptors being reduced or oxidized.
- Typically, the time constant associated with this process is ~10 ms.
Generation Time

- Specifically, we can say that on average that it takes a time a time $\tau_g$:
- It turns out, that in order for the inversion charge to be generated, we require a sufficiently slow rate of change of voltage:

$$\frac{dV}{dt} \leq \frac{qn_iW}{\tau_g C_i} \quad (9)$$
- Symbols take their usual meaning.

Inversion Non-Idealities

- For silicon, at $T = 300K$ and $n_i = 10^{10} \text{ cm}^{-3}$:
  - If $d = 5\text{nm}$, $W = 1 \mu\text{m}$ and $\tau_g = 10 \mu\text{s}$:

$$\frac{dV}{dt} \leq 0.023 \text{ V/s}$$

  - If $d = 5\text{nm}$, $W = 1 \mu\text{m}$ and $\tau_g = 1 \text{ ms}$:

$$\frac{dV}{dt} \leq 0.23 \text{ mV/s}$$
Low-Frequency
• So the behavior we observe depends strongly on the frequency at which we carry out the measurement.
• At low frequencies, we expect both the dielectric relaxation and minority carrier generation to be in equilibrium.
• So under these circumstances we will have inversion as we expect.

Capacitance-Voltage Plot
• So at low frequencies, the capacitance recovers back to a similar value for accumulation:

\[ C_{\text{inv,lf}} = C_i \]  \hspace{1cm} (10)
• Back to our diagram:
Low Frequency

• We expect that the capacitance will reach a minimum at inversion and then begin to retrace to the insulator capacitance.

• This is because at inversion the depletion region width reaches a maximum:

\[ W_{\text{max}} = \sqrt{\frac{2\varepsilon_0 \varepsilon_{rs} \phi_s (\text{inversion})}{e N_A}} \]  \hspace{1cm} (11)

• Or, at the onset of strong inversion \((\phi_s = 2\phi_{Bp})\):

\[ W_{\text{max}} = \sqrt{\frac{4\varepsilon_0 \varepsilon_{rs} \phi_{Bp}}{e N_A}} \]  \hspace{1cm} (12)

High-Frequency

• At higher frequencies however we expect only the dielectric relaxation to have completed in the AC voltage cycle.

• I.e. during the AC cycle, not enough time has passed for electrons (in this case) to be generated.

• In this case, we are just at simple depletion, as we saw previously.
Capacitance-Voltage Plot

• So at high frequencies, the capacitance is similar to as if we had stayed at depletion.

\[ C_{\text{inv,hf}} = \frac{C_D C_i}{C_i + C_D} \]  \hspace{1cm} (13)

High Frequency

• At higher frequency, the capacitance saturates at:

\[ \frac{1}{C_{\text{inv,hf}}} = \frac{W_{\text{max}}}{\epsilon_0 \epsilon_{rs}} + \frac{1}{C_i} \]  \hspace{1cm} (14)

• This minimum capacitance is achieved because although the depletion layer charge can keep up with the AC signal, the inversion layer charge cannot.
Deep Depletion

- Finally, let us consider one more possibility.
- Remember how we actually measure capacitance.
  - Can charge or discharge a capacitor through a known resistance, and measuring the resulting rate of change in voltage:

\[ I(t) = C \frac{dV}{dt} \]  

(15)

- Hence time-dependence is an inherent part of a capacitance measurement.

Deep Depletion

- In reality we would use an impedance analyzer and measure the attenuation of either a low-pass or high-pass filter as a function of applied frequency.
Deep Depletion

• When we are measuring our MOS capacitors we are doing this, but we are also applying a DC bias across the device.

Sine wave, typically $f = 1$ MHz, $V_{AC} = 25$ mV (rms)

$V_{DC} = 0$-$10$ V

• Up until now we have been talking about the frequency of small AC signal.

Deep Depletion

• But in reality we also must scan the DC voltage to produce our $CV$ curve.

• So in reality our voltage-time graph will look something like the following:

$V$ vs. $t$
Deep Depletion

- Deep depletion occurs when we ramp our DC voltage too quickly.
- Under these circumstances the charge distribution is unable to come to equilibrium and the depletion width increased beyond its maximum depletion width (i.e. > $W_{\text{max}}$).
- We are not going to quantify this behavior, but mention it for completeness.

CV Plot (Sze & Ng).

- The textbook shows the same behavior we have talked about:
Flatband Voltage

- You may find the voltage at which the $CV$ curve makes the transition from accumulation-depletion is not always zero:
Flatband Voltage

- This is due to the presence of trapped charges / impurities in the oxide / semiconductor / interface.
- Trapped charges have the effect of making the system behave as if a potential is already being applied.
- You need to overcome this potential to return the system to a neutral state.
- Analogous to the threshold voltage in a transistor.
- In a $CV$ curve this is manifest in as a rigid shift in the characteristics along the voltage axis, by a fixed amount.

\[ V_{FB} = \phi_{MS} - \frac{Q_F}{C_i} - \gamma M \frac{Q_M}{C_i} - \gamma OT \frac{Q_{OT}}{C_i} - \frac{Q_{IT}(\phi_S = 0)}{C_i} \]  

- Where each of the terms are due to some insulator charge.
Flatband Voltage

- We characterize this shift by the voltage $V_{FB}$:

$$V_{FB} = \phi_{MS} - \frac{Q_F}{C_i} - \gamma_M \frac{Q_M}{C_i} - \gamma_{OT} \frac{Q_{OT}}{C_i} - \frac{Q_{IT}(\phi_s = 0)}{C_i} \tag{16}$$

- $V_{FB}$ = flatband voltage.
- $\phi_{MS}$ = metal-semiconductor work function difference.
- $Q_F$ = fixed oxide charge. $Q_M$ = mobile ion charge.
- $Q_{OT}$ = oxide trapped charge.
- $Q_{IT}(\phi_s = 0)$ = interface trapped charge (evaluated at a surface potential of zero, i.e., flatband).

Flatband Voltage

- We characterize this shift by the voltage $V_{FB}$:

$$V_{FB} = \phi_{MS} - \frac{Q_F}{C_i} - \gamma_M \frac{Q_M}{C_i} - \gamma_{OT} \frac{Q_{OT}}{C_i} - \frac{Q_{IT}(\phi_s = 0)}{C_i} \tag{16}$$

- The two $\gamma$'s are charge centroid factors which are given by:

$$\gamma_j = \frac{\int_0^d x \frac{d}{dx} \rho_j(x) dx}{\int_0^d \rho_j(x) dx} \tag{17}$$

- $j = M$ for mobile charges.
- $j = OT$ for oxide-trapped charges.
Flatband Capacitance

- Before you can assess the flatband voltage, you need to know the corresponding flatband capacitance.
- The flatband capacitance \( C_{FB} \) is defined as:
  \[
  C_{FB} = \frac{\varepsilon_r \varepsilon_0}{L_D}
  \]  
  (18)
- Where \( L_D \) is the Debye Length:
  \[
  L_D = \sqrt{\frac{k_B T \varepsilon_r \varepsilon_0}{p_{p0} e^2}}
  \]  
  (3)

Normalized \( C_{FB} \)

- We can normalize the flatband capacitance to the oxide capacitance with these empirical expressions:
  - P-Type:
    \[
    \frac{C_{FB}}{C_{ox}} = \left[ 1 + \frac{136 \sqrt{T/300}}{d \sqrt{N_A}} \right]^{-1}
    \]  
    (19)
  - N-Type:
    \[
    \frac{C_{FB}}{C_{ox}} = \left[ 1 + \frac{136 \sqrt{T/300}}{d \sqrt{N_D}} \right]^{-1}
    \]  
    (20)
- This is only valid for \( d \) in cm, \( N_D \) or \( N_A \) is in cm\(^{-3}\), and \( T \) in K.
Normalized $C_{FB}$

- Plotted as a function of $d$:

![Normalized Capacitance Graph](image)

**Insulator Charge**
Insulator Charge

- So it turns out that the main deviations from ideal MOS behavior are associated with insulator charge - charges in the oxide or at the oxide/semiconductor interface.
- We focus on the technologically important SiO₂/Si interface.
- But many arguments are general.

Insulator Charge

- We are going to talk about 4 types of charges that lead to non-idealities.

Fixed oxide charge

Mobile ionic charge

Trapped oxide charge

Interface trapped charge

SiO₂

silicon

Q_{IT}
1. Fixed Oxide Charge

- Start with fixed charges in the oxide (SiO$_2$):

![Diagram showing fixed oxide charge close to SiO$_2$/Si interface.]

- These are positively charged (+).
- Have a two-dimensional charge density labeled by: $Q_F$.
- Located $\lesssim 30$ nm from the SiO$_2$/Si interface.

- Cannot be charged or discharged by varying the surface potential.
- Density is not a function of doping type, doping density, or oxide thickness.
- Does depend on substrate orientation, oxidation temperature and ambient, and post-oxidation anneal conditions.
- Formation mechanism is debated. Probably due to nonstoichioimetric SiO$_2$ near the interface (excess Si, nonbridging O,...).
1. Fixed Oxide Charge

- $Q_F = 10^{10}-10^{12} / \text{cm}^2$, dependent upon the final oxidation or annealing treatment.
- Flatband voltage due to fixed oxide only:
  \[ V_{FB} = -\frac{Q_F}{C_i} \]  
  (21)
- This assumes the charge distribution is a delta-function:
  \[ Q_F(x) = Q_F \delta(x) \]  
  (22)
- Where $\delta(x)$ is the Dirac delta function.

2. Mobile Ions

- Mobile ionic charge in the SiO$_2$: Labelled in Equation (16) by $Q_M$.
- Usually due to positively charged alkali impurity ions, such as Na$^+$, K$^+$, Li$^+$. 
2. Mobile Ions

- Historically, this was a severe problem because it led to device instabilities and reproducibility problems associated with the variable amount and physical location of the mobile impurities.
- Encapsulation with silicon nitride, borophosphosilicate glass (BPSG & PSG), aluminum oxide, etc., can minimize this problem.
- Cl treatments (HCl, ...) during oxidation or to the oxidation furnace can help eliminate this problem.

$$\gamma_M = \frac{\int_0^d x \rho_M(x) dx}{\int_0^d \rho_M(x) dx}$$  (24)

2. Mobile Ions

- It is not physical to describe the mobile ionic charge density as a delta function unfortunately.
- Flatband voltage due to mobile ions only:
  $$V_{FB} = -\gamma_M \frac{Q_M}{C_i}$$  (23)
- We encapsulate the non-homogenous distribution through the charge centroid function for mobile ions:
  $$\gamma_M = \frac{\int_0^d x \rho_M(x) dx}{\int_0^d \rho_M(x) dx}$$  (24)
- $$\rho_M(x)$$ is 3-dimensional charge density of mobile ions.
2. Mobile Ions

\[ \gamma_M = \frac{\int_0^d x \rho_M(x) dx}{\int_0^d \rho_M(x) dx} \]  

- The charge centroid function takes account of the fact that charge at the Si/SiO\(_2\) interface will have a greater impact on \(V_{FB}\) than charge deeper in the oxide.
- Charge at the metal/SiO\(_2\) interface, \(x = 0\), will have no impact (~as if the charge was in the metal).

3. Oxide Trapped Charge

- More trapped charges in the oxide.
- Similar phenomenologically to 1: \(Q_F\).
- However we label this \(Q_{OT}\).
- Ionizing radiation with an energy greater than the SiO\(_2\) bandgap (~9 eV) creates e\(^-\)/h\(^+\) pairs in the oxide.
3. Oxide Trapped Charge

- Holes can be captured by a normally neutral hole trap near the interface (especially when the gate voltage is positive).
- These (deep) traps remain charged after the ionizing radiation ends.
- Can also be generated during various processing steps which employ high energy radiation (electron beam processing, ion implantation, x-ray processing, etc.).
- This type of charge can be annealed out at ~300ºC.

\[ V_{FB} = -\gamma_{OT} \frac{Q_{OT}}{C_i} \]  
(25)

Where we once again use a centroid function to describe distribution (c.f. fixed oxide charge which is described by a delta function):

\[ \gamma_{OT} = \frac{\int_0^d x \rho_{OT}(x)dx}{\int_0^d \rho_{OT}(x)dx} \]  
(26)

- \( \rho_{OT}(x) \) is 3-dimensional charge density of oxide trapped charge.
3. Oxide Trapped Charge

- Interface traps ($Q_{IT}$ - number 4) are produced simultaneously with $Q_{OT}$.
- Structure: oxygen vacancy sites in the SiO$_2$ density determined by thermodynamics (Gibbs free energy of vacancy formation).
- Oxide traps are not much of a concern in MOSFET gate insulators below ~5 nm thickness.
- However, oxide traps are still a concern in "parasitic" insulators such as field oxides and buried oxides in SOI (silicon on insulator) technologies.

4. Interface Traps

- Labeled $Q_{IT}$.
- Located right at the Si/SiO$_2$ interface.
- The charge state depends on the position of Fermi level; interface states can be charged or discharged by the application of an appropriate bias.
4. Interface Traps

- $Q_{IT}$ may be reduced by a low temperature (~300-500°C) anneal in a hydrogen containing ambient; 'hydrogen ties up dangling bonds'.
- $Q_{IT}$ may be reduced to $\sim 10^{10}$ cm$^{-2}$ (i.e. about one trap for every $10^5$ surface atom).
- Traps can be positively or negatively charged (i.e. donor- or acceptor-like).
- The best way to cope with this issue is to think about charge balance and to introduce the idea of a charge neutrality level and a neutral Fermi-level position.

- We can encapsulate this behavior in a similar approach we took when talking about surface states in metal-semiconductor contacts (Lecture 9):
  - The states are classified relative to the Charge Neutrality Level ($E_{CNL}$).
  - **Acceptor-like states** are neutral when empty and negatively charged when occupied.
  - **Donor-like states** are positively charged when empty and neutral when occupied.
4. Interface Traps

- The textbook pictures it like so:

Fig. 13 Any interface-trap system consisting of both acceptor states and donor states can be interpreted by an equivalent distribution with a neutral level $E_n$ above which the states are of acceptor type and below which is donor type. When $E_F$ is above (below) $E_n$, net charge is $-+$. (Sze & Ng Fig. 4.7, pg. 206)

- Recall we are here talking about semiconductor-insulator (oxide) interface rather than metal-semiconductor interface.
- Yet the theory on trap states is general.

As these states are located at one position only, we can describe them with a delta function and hence just say:

$$V_{FB} = -\frac{Q_{IT}(\phi_s = 0)}{C_i}$$

(27)

- Note:
  - $Q_{IT}(\phi_s = 0)$ = interface trapped charge (evaluated at a surface potential of zero).
  - So while the contribution to the flat band voltage is evaluated for when $\phi_s = 0$, the density of interface charge $Q_{IT}$, is bias dependent.
MOSFETs

- This is not a course on field-effect transistors, but the behavior of MOS capacitors is relevant to their study.

- Carriers travel at interface between semiconductor and dielectric

MOSFETs

- Insulator charge is hence very important in MOSFETs.
- Charge present at or near the SiO₂/Si interface results in an additional scattering mechanism for inversion channel carriers traveling lateral to this interface. This lowers the mobility of these carriers.
- The carriers induced in inversion (if inversion-mode FET) layers by \( V_G \) may be trapped in interface states, lowering the number of carriers available for contributing to the current and, thus, lowering the current, conductance, and transconductance.
MOSFETs

- If carriers in the inversion layer are subjected to a large enough field, they can get ‘hot’ and may even gain enough energy to be injected into the insulator conduction band or valence band.
- Some of these carriers may be trapped in deep oxide traps, resulting in a shift in the MOSFET threshold voltage and also may lead to additional trap state formation.
- The carriers that are injected into the insulator and transit to the gate are simply lost to conduction.

Bias-Temperature Stressing
Bias-Temperature Stressing

• If you do something to the MOS capacitor to change the flatband voltage (by $\Delta V_{FB}$), this can be used to estimate an effective charge ($Q_{eff}$).

$$Q_{eff} = -\Delta V_{FB} C_i$$  \hspace{1cm} (28)

• This assumes that all of the charge is present at the interface (thus implying $\gamma = 1$).
• This idea is used in the bias-temperature stress method to determine the mobile ion charge.

Bias-Temperature Stressing

• To accomplish this measurement, heat the device up to $\sim 150$-$250^\circ$C, apply a positive voltage (oxide field $\sim 1$ MV cm$^{-1}$) for $5$-$10$ minutes, cool the sample down, and measure the flatband voltage.
• Repeat this for a negative gate voltage.
• If all of the mobile charge is sufficiently mobile, then $\gamma_m = 0$ for the one polarity and $\gamma_m = 1$ for the opposite polarity.
• Oxide trapped charge can be similarly investigated by monitoring the flatband voltage as a function of radiation dose.
Bias-Temperature Stressing

• Although there are ways to measure the charge distribution in the oxide (e.g., etch-off and photo IV methods), $\gamma = 1$ is usually assumed for these measurements.

• $CV$ curves sometimes exhibit hysteresis, in which curves do not retrace themselves when sweeping in a forward and a reverse direction.

![Graph showing bias-temperature stress]

• We know that in reality, $V_{DC}$ is not DC, it will be some sort of triangle wave, just with a very slow frequency.

![Graph showing bias-temperature stress with triangle wave]

ECE 615 – Semiconductor Devices I
Winter 2019 - John Labram
Bias-Temperature Stressing

- The **triangular voltage sweep** method is an alternative to the bias-stress measurement for estimating mobile charge density.
- In this method, both high- and low-frequency C-V curves are obtained at an elevated temperature of ~150-250 °C.
- Recall, for inversion to occur we needed generation to take place fast enough:
  \[
  \frac{dV}{dt} \leq \frac{qn_i W}{\tau_g C_i} \quad (9)
  \]
- At higher \( T \), the generation time \( \tau_g \) decreases.

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Bias-Temperature Stressing

- What we observe is something like the following:

![Image](image_url)

- So, because of the elevated temperature, we are observing inversion behavior **even at high-frequencies**.
Bias-Temperature Stressing

- What about at low frequencies?

\[ C \]

\[ V \]

- This is a rather unexpected behavior can occur.
- It is due to mobile ions.

Recall we mentioned there are a number of mobile charges in our capacitor.
Bias-Temperature Stressing

- The mobility of ionic species is positively correlated with temperature.
- Typically derived by some temperature-activated Arrhenius relationship:

\[
\mu_{\text{ion}} = \mu_{\text{ion}}^{(0)} \exp \left( -\frac{E_A}{k_B T} \right)
\]  

(29)

- At high-enough temperatures some ionic species (e.g. Na\(^+\) or K\(^+\)) will become mobile.

Bias-Temperature Stressing

- The mass of ions is about \(10^4 \text{ – } 10^5\) times higher than electrons (and holes).
- So they take a long time to respond to applied fields.
Bias-Temperature Stressing

- Under certain conditions:
  - Temperature.
  - DC voltage.
  - DC sweep rate.
  - Resonance can occur, and charges will be in phase with applied voltage:

![Diagram showing resonant peaks](#)

- AC voltage.
- AC frequency.

This can lead to spikes in capacitance at certain voltages:

![Graph showing capacitance variation](#)

Figure 6.19 Schroeder
Summary

- We looked at “ideal” CV curves:

![CV Curves Diagram]

- The how oxide charges can effect measurements:

![Oxide Charges Diagram]

Next Time…

- We will begin our study of heterostructures

![Heterostructures Diagram]