\[ i(t) = C \frac{dv}{dt} \]

**Power from gen.** \( E_g i(t) \)

**Energy from gen.**

\[
E = \int_{v(0)}^{v(\infty)} E_g C \left( \frac{dv}{dt} \right) dt = EC \int_{v(0)}^{v(\infty)} dv = CE_g^2
\]

Twice the energy stored in \( C \)!

**Analysis:**

\[
E_g \frac{1}{s} = \mathcal{L} \left\{ R + \frac{1}{sC} \right\} \Rightarrow \mathcal{L} \{ i(s) \}
\]

\[
i(t) = \left( \frac{E_g}{R} \right) e^{-t/RC}
\]

**Power in \( R \):** \( i^2(t)R \)

**Energy lost in \( R \):**

\[
E_R = \int_{0}^{\infty} i^2(t)R \, dt = CE_g^2/2
\]
Re: graphs; CAD

From: "Kartikeya Mayaram" <karti@eeecs.oregonstate.edu>
To: <eeecs-grads@engr.orst.edu>
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Sent: Tuesday, September 21, 2010 6:15 PM
Subject: Fall 2010 New Graduate Course: Analog Circuit Simulation

ECE 521 - Analog Circuit Simulation - Fall 2010 (MW 2-3:50pm)

How this course adds to the curriculum?

This course supplements other courses in the circuit design area such as ECE 4/522, ECE 4/523, ECE 520. Students use the circuit simulator SPICE extensively in these courses but are not aware of the theoretical and practical aspects of building a circuit simulator such as SPICE. This course provides them with an understanding of the key issues and also provides a stronger foundation in circuit theory and numerical methods. Essentially, this course addresses "Everything you wanted to know about SPICE but were afraid to ask!"

When/Where
Fall 2010: MW 2-3:50pm (Room TBD)

Prerequisites
A background in circuit theory, ability to write software in (C, C++, or Fortran), and an appreciation for numerical methods

Topics
1. Formulation of circuit equations using the following methods: nodal analysis (NA), modified nodal analysis (MNA), and sparse tableau approach (STA)

2. Solution of linear equations with direct and iterative methods and sparse-matrix solution techniques

3. DC analysis of circuits and solution of nonlinear equations and convergence issues

4. Small-signal ac, transient, sensitivity, noise, and pole/zero analyses

5. Analysis methods for RF circuits
Instrumentation amplifier

Note the very high-resistance $R_{\text{bogus}_1}$ and $R_{\text{bogus}_2}$ resistors in the netlist (not shown in schematic for brevity) across each input voltage source, to keep SPICE from thinking $V_1$ and $V_2$ were open-circuited, just like the other op-amp circuit examples.

**Netlist:**

```plaintext
Instrumentation amplifier

v1 1 0
r1 0 2 1k
v2 4 0 dc 5
v3 4 0 dc 5
v4 6 0 dc 5
v5 6 0 dc 5
v6 8 0 dc 5
rload 9 0 10k
r1 2 3 10k
rgain 2 5 10k
r2 5 6 10k
r3 3 7 10k
r4 7 9 10k
r5 6 8 10k
r6 8 0 10k
.dc v1 0 10 1
.print dc v(9) v(3,6)
.end
```