

ECE 627 PROJECT

Design of a Delta-Sigma A/D Converter

Due: June 5, 2015

Design a delta-sigma ($\Delta\Sigma$) ADC for the following specifications:

Signal bandwidth	0 – 500 kHz
Clock frequency	Less than 200 MHz
Accuracy	At least 17 bits

Design tasks:

1. Choose an architecture. Justify your choice in terms of performance, power dissipation, complexity, etc.
2. Carry out the theoretical design: find the STF and NTF, draw the block diagram in terms of delay elements, adders, comparators, DACs, etc.
3. Plot the pole-zero patterns, and the NTF and STF gain-frequency curves.
4. Simulate the SNR vs. input sine-wave amplitude characteristics.
5. Perform scaling for optimum dynamic range performance.
6. Design and draw the switched-capacitor realization of the ADC loop, considering the kT/C noise.
7. Simulate the switched capacitor realization in SWITCAP or other CAD tool.
8. Find the minimum slew rate needed by the opamps when the output is allowed to slew only for 20% of the settling time available.
9. Design and draw a decimation filter to follow the $\Delta\Sigma$ loop.
10. Simulate the overall performance of the complete ADC in MATLAB.
11. Analyze and describe the nonideal effects influencing the performance: finite opamp gain, finite opamp bandwidth, slew rate, capacitor mismatch, analog noise, digital round-off errors, etc

The report must be typed and short (5-6 pages maximum, not counting the Appendix). It must contain a table with achieved performance, including the total capacitance value (after optimization), an Appendix with the MATLAB code, and any netlists used for circuit simulations.