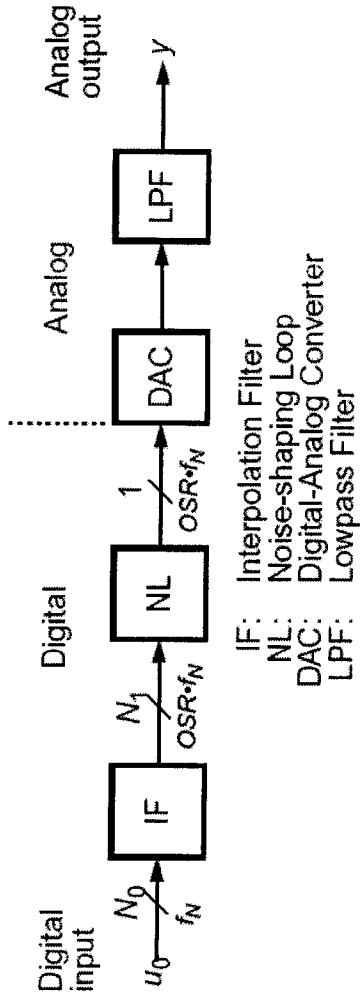
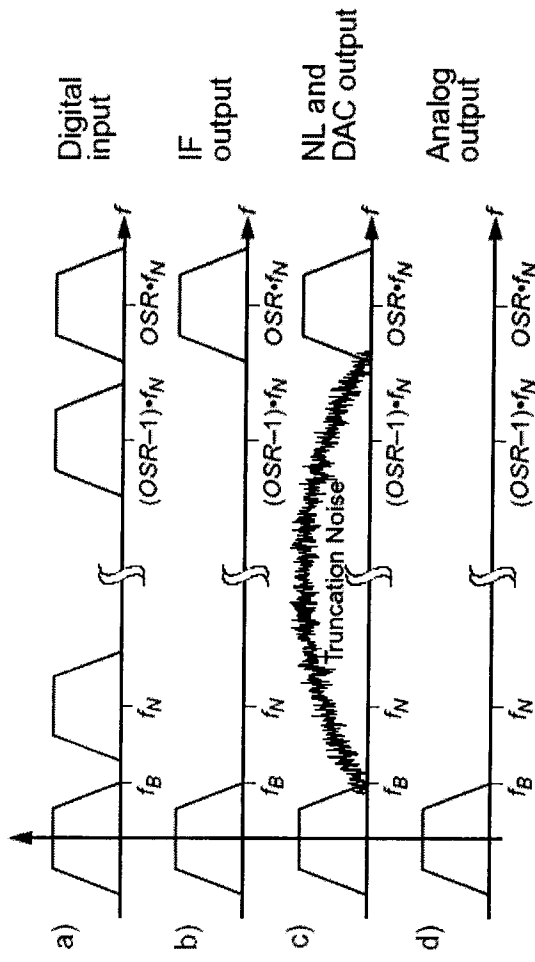


$\Delta\Sigma$ DAC STRUCTURE



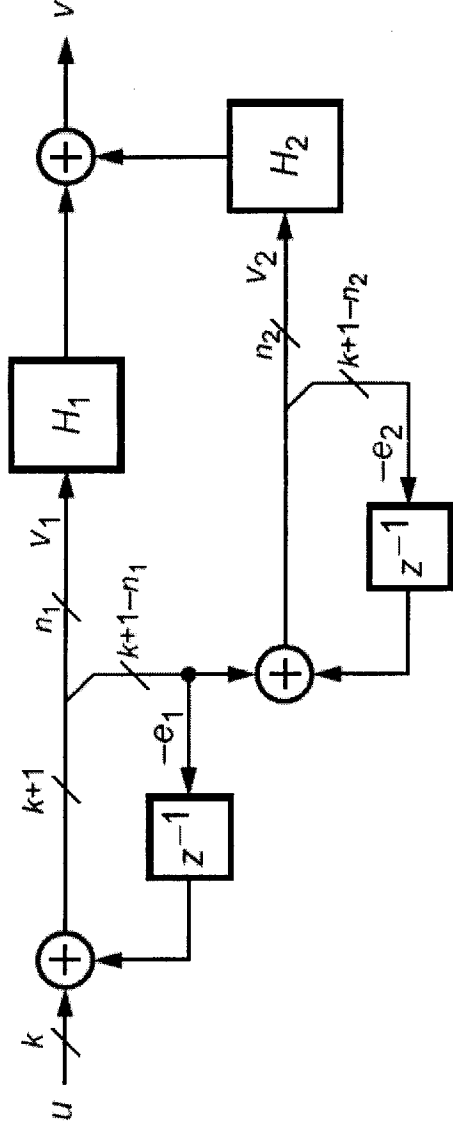
Block diagram of a $\Delta\Sigma$ DAC.

Single-bit DAC can be linear. For a few bits (2~4), DEM can be used

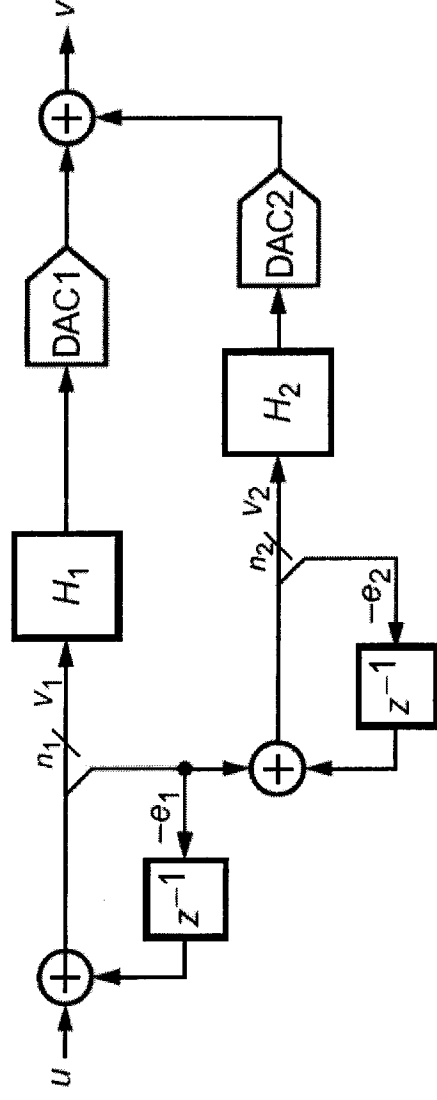


Signal and noise spectra in a $\Delta\Sigma$ DAC.

CASCADE DACS

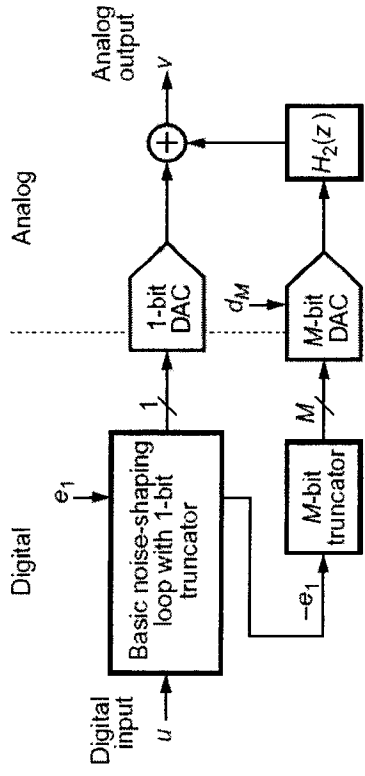


Cascade structure for a second-order noise-shaping loop.

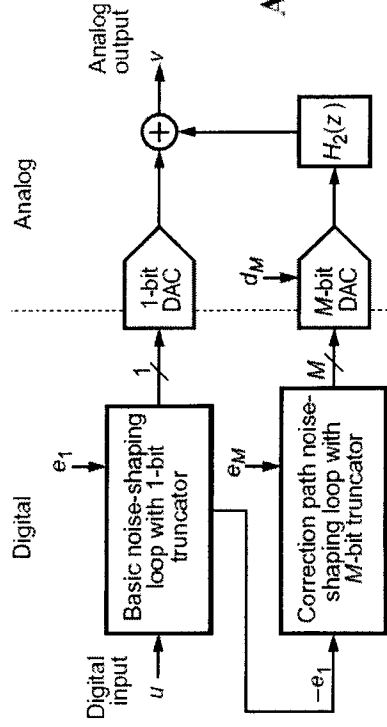


A cascade DAC using analog recombination.

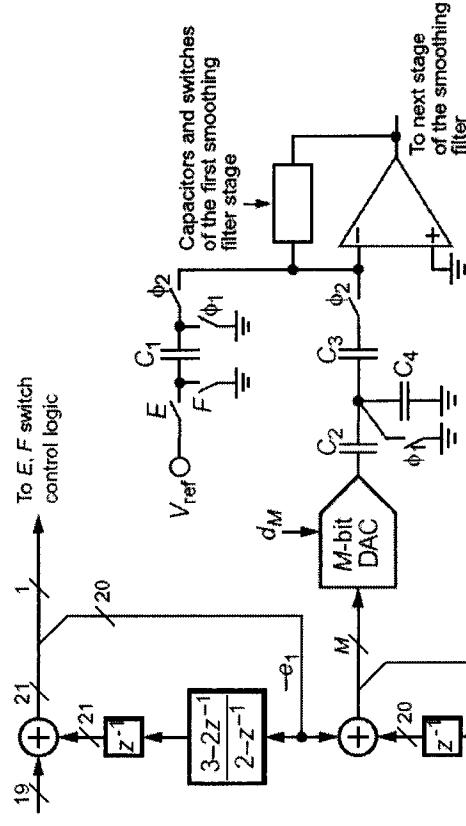
DUAL TRUNCATION DACS



A dual-truncation DAC system.

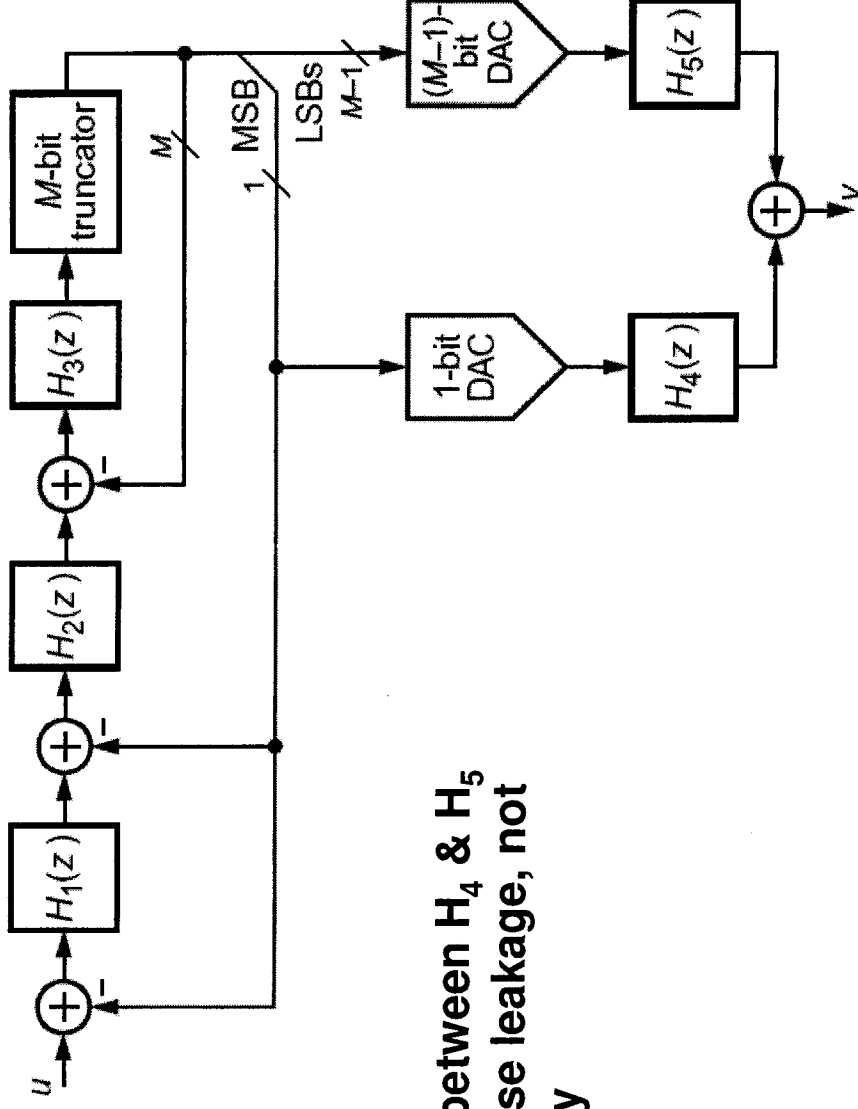


A dual-truncation MASH structure.



A third-order dual-truncation MASH noise-shaping stage.

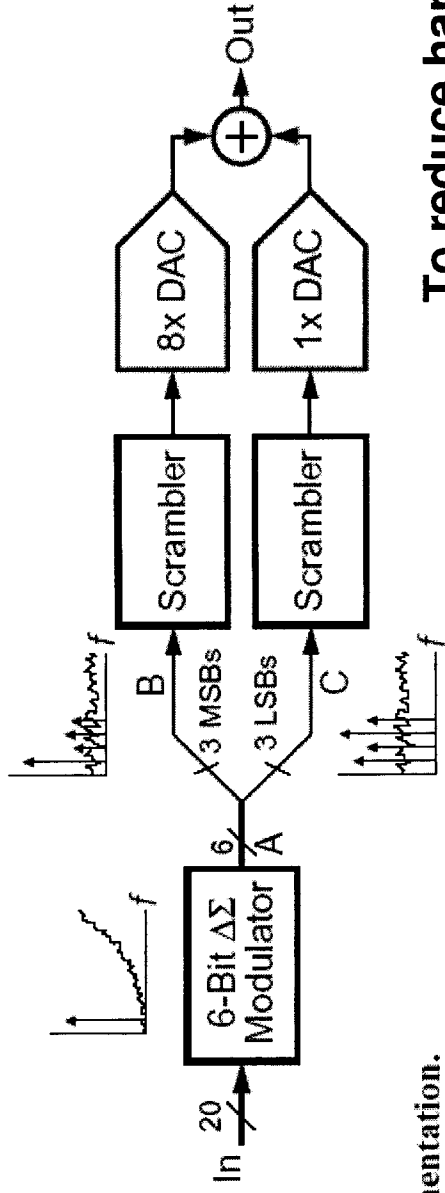
HARAPETIAN'S SCHEME



Mismatch between H_4 & H_5
causes noise leakage, not
nonlinearity

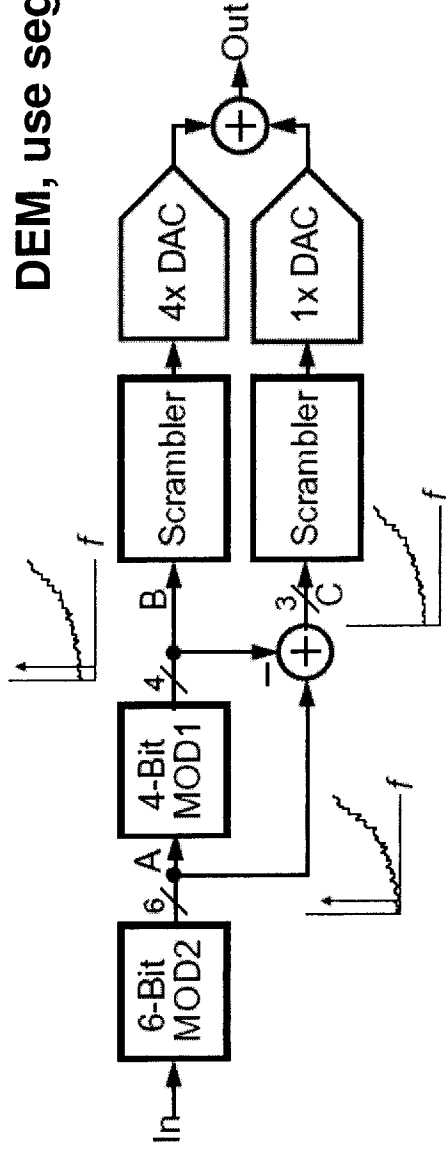
A single-stage dual-truncation D/A loop.

SEGMENTED DACS



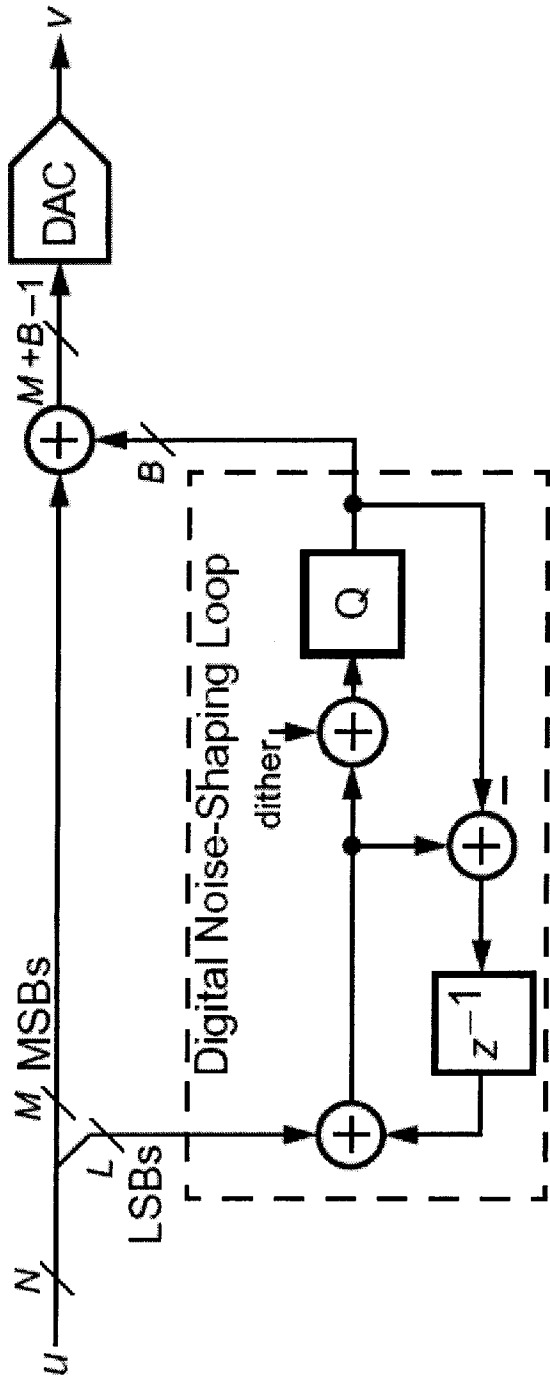
Segmentation.

To reduce hardware needed in the DAC and the DEM, use segmentation



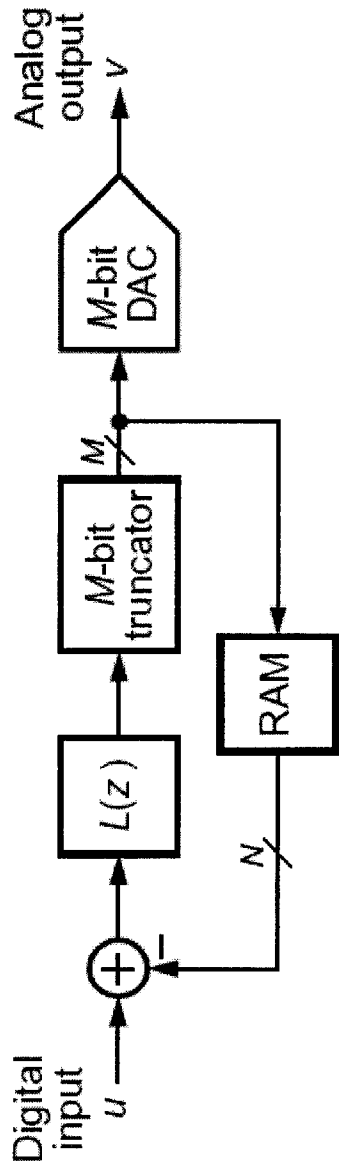
Noise-shaped segmentation.

ANOTHER SEGMENTATION SCHEME

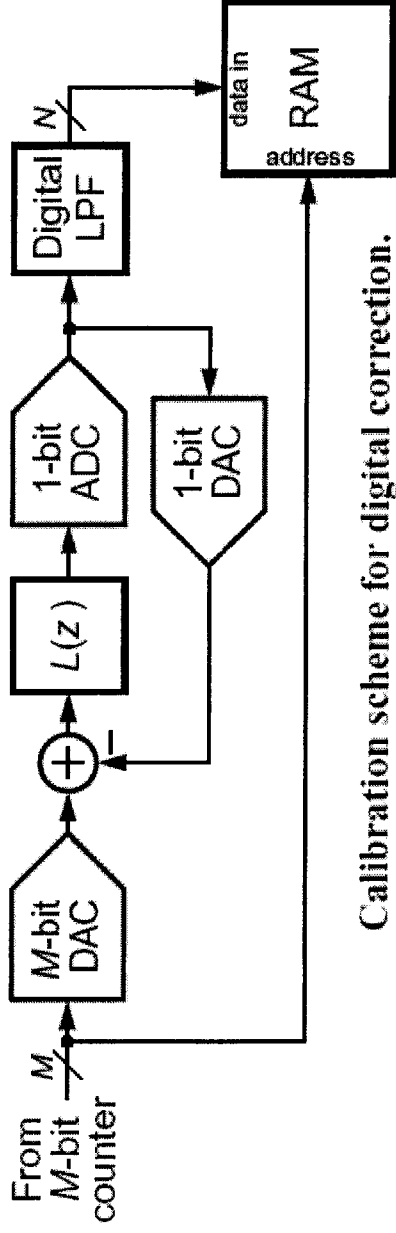


A hardware-reduced first-order modulator with dither.

A POWER-UP CORRECTION METHOD



A digitally-corrected M -bit DAC.



Calibration scheme for digital correction.

COMPARISON OF SINGLE- AND MULTI-BIT $\Sigma\Delta$ DACS

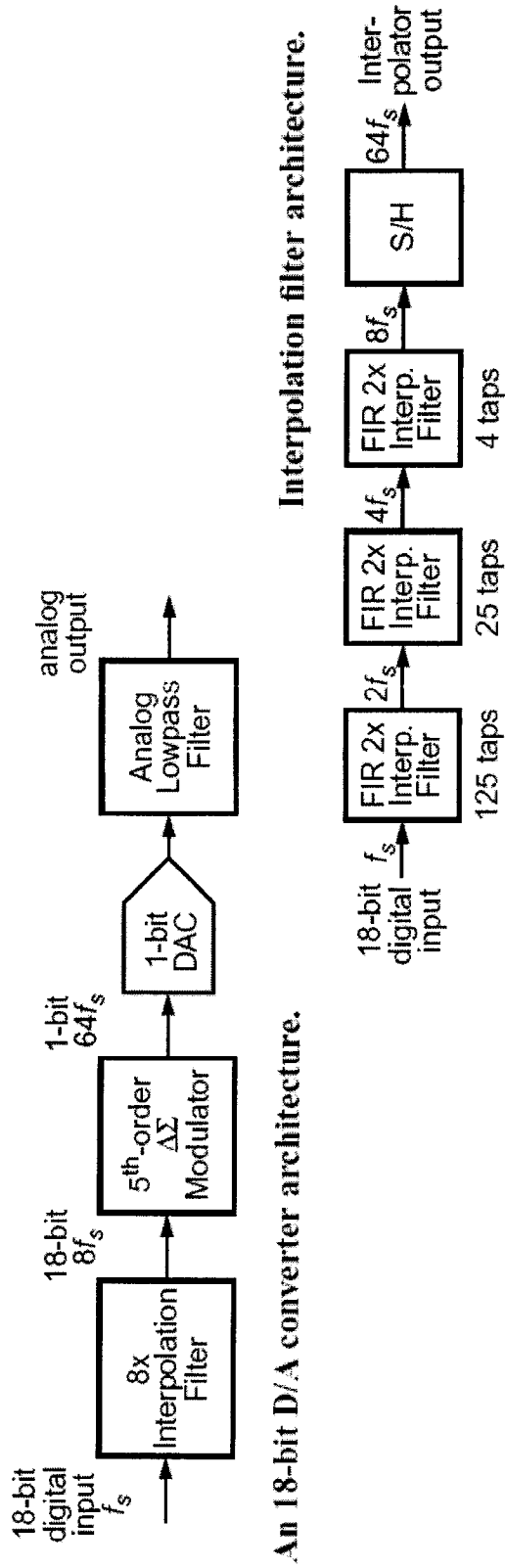
Single-bit truncation: Much simpler internal DAC structure can be used, without the need for thermometer coding, unit elements and digital mismatch-shaping logic.

Multi-bit truncation: Several advantages can be obtained, including

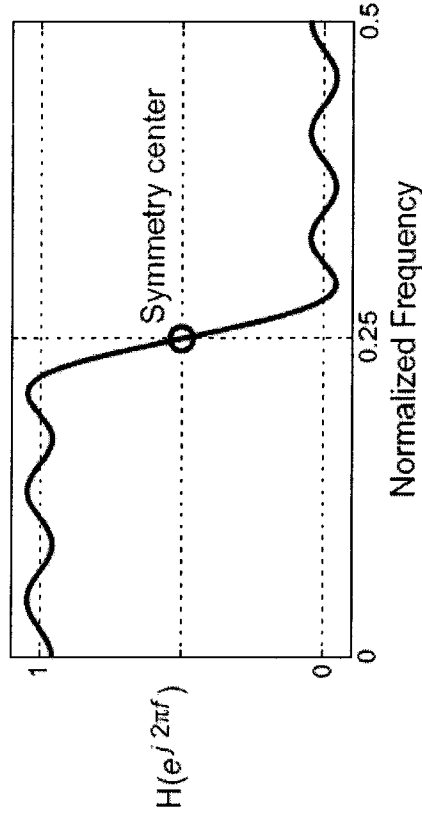
1. Simpler digital noise-shaping loop, since more aggressive NTF may be used, and since the truncation noise is reduced by at least $N - 1$ bits.
2. Less (or no) dithering, since tones are less likely to be generated, and since typically the amplitude of dithering is about $1/2$ LSB, which is smaller in a multi-bit quantizer.
3. Much simpler analog smoothing filter, since the slewing and out-of-band noise in the DAC output are both reduced. Also, the sensitivity to clock jitter is reduced, due to the reduced step size in the DAC output signal.[†]

Generally, the advantages of multi-bit truncation outweigh those of single-bit truncation, and hence it is preferable to design $\Delta\Sigma$ DACs with multi-bit internal DACs.

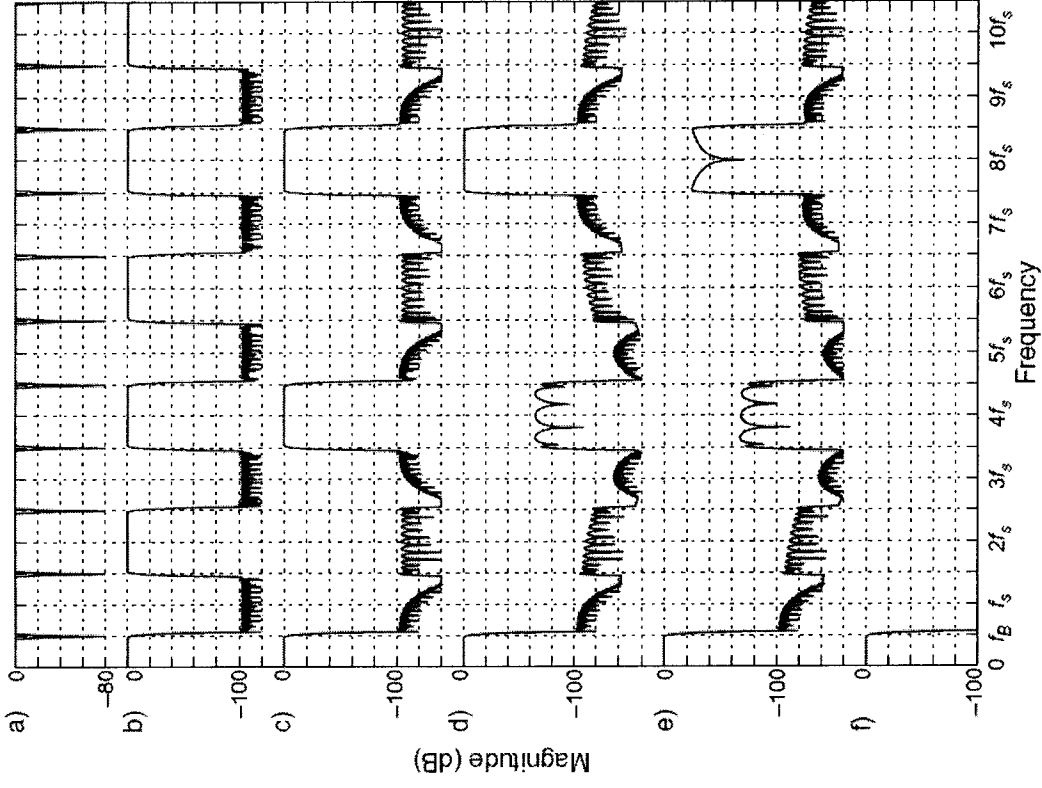
AN EXAMPLE [3]



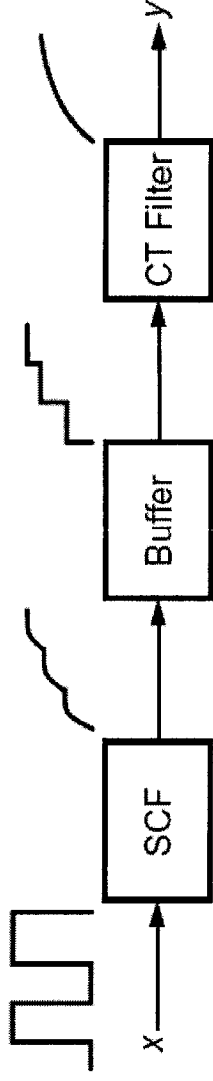
Frequency response of a half-band filter.



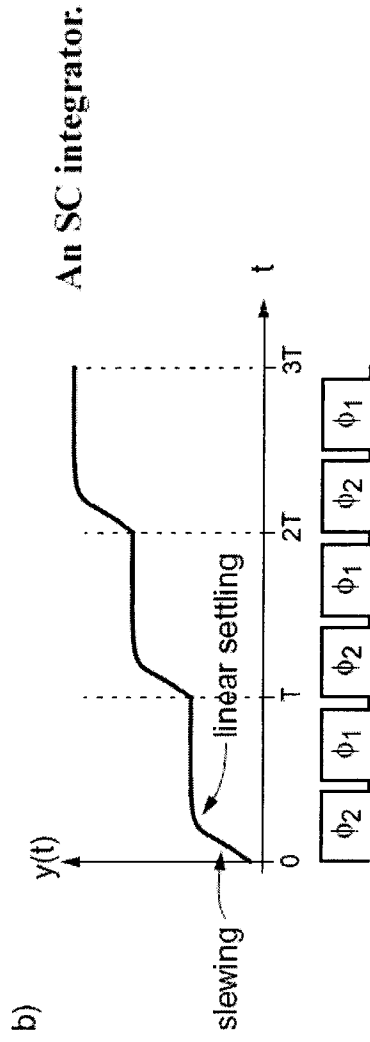
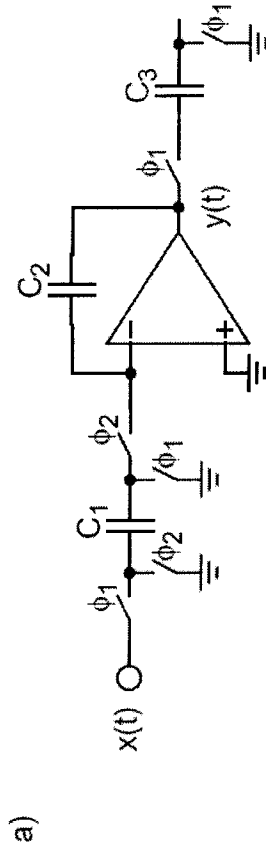
SPECTRA WITHIN $\Delta\Sigma$ DAC SYSTEM



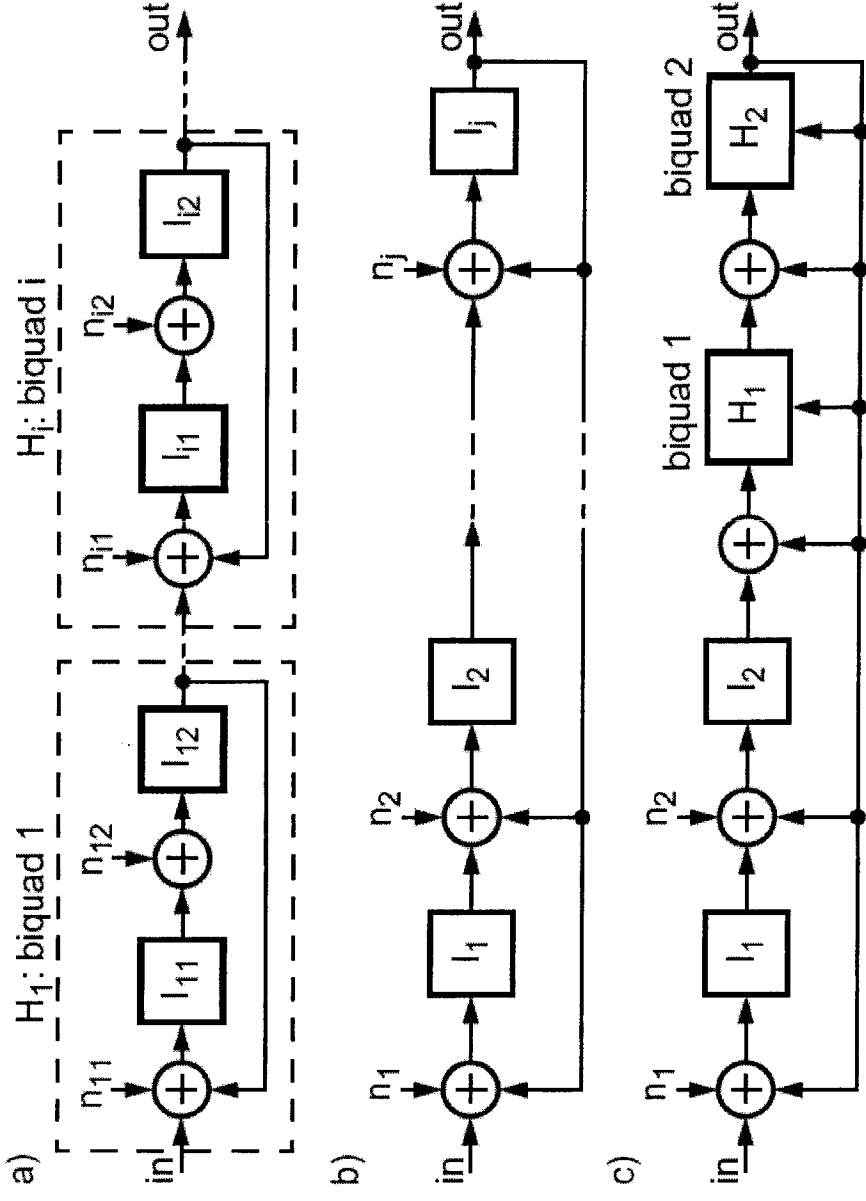
POST-FILTER DESIGN



Post-filter for a 1-bit $\Delta\Sigma$ DAC and associated signals.

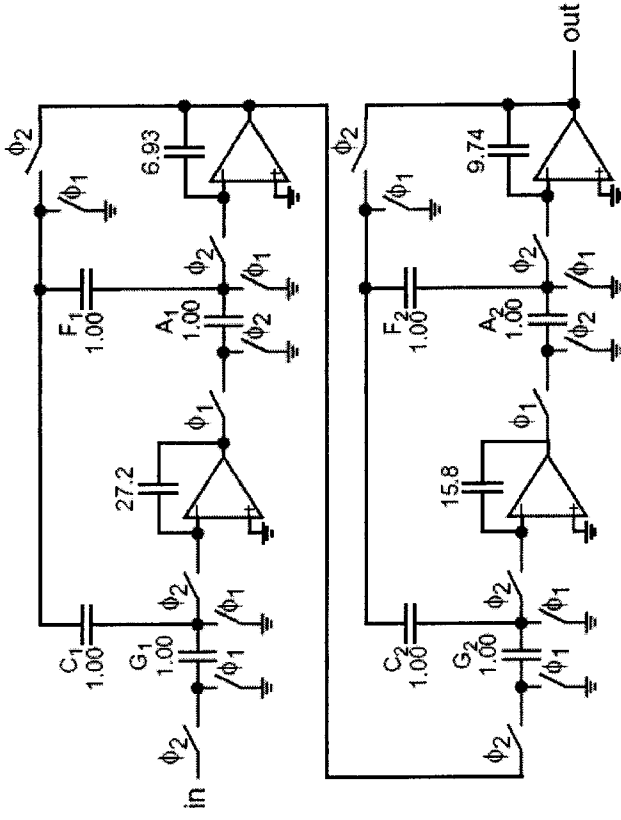


RECONSTRUCTION FILTER ARCHITECTURES

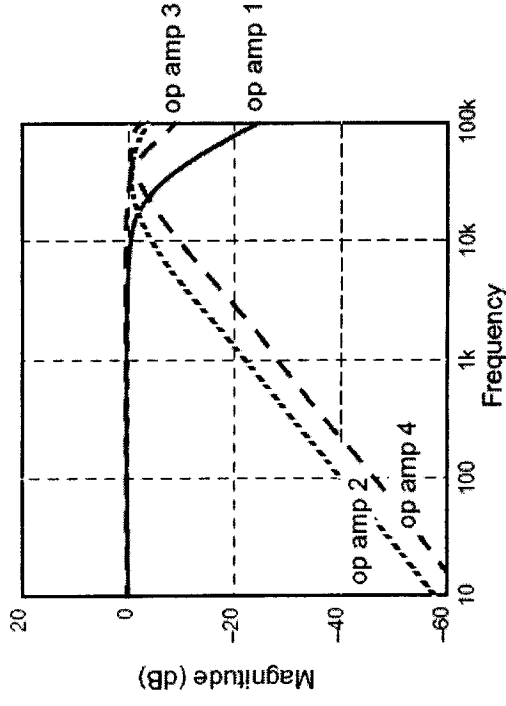


POST-FILTER EXAMPLES (1)

A 4th-order Bessel filter implemented with a cascade of biquads.

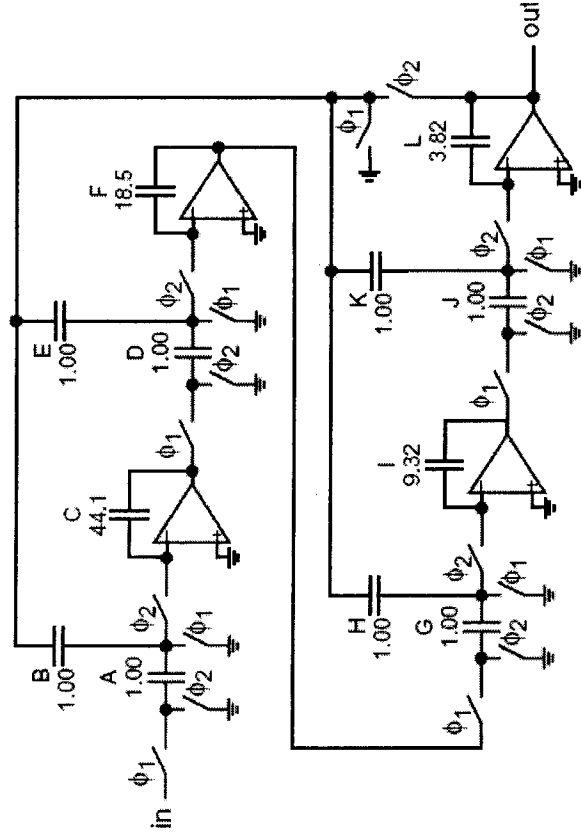


Noise gains from each op-amp input

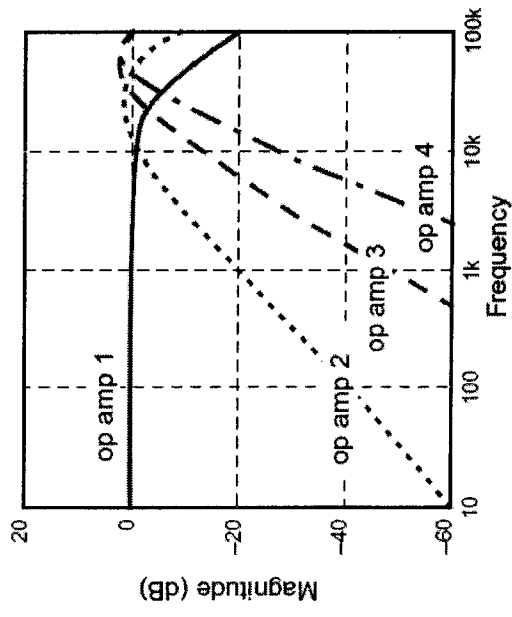


POST-FILTER EXAMPLES (2)

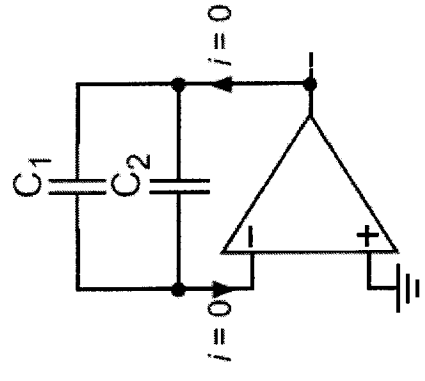
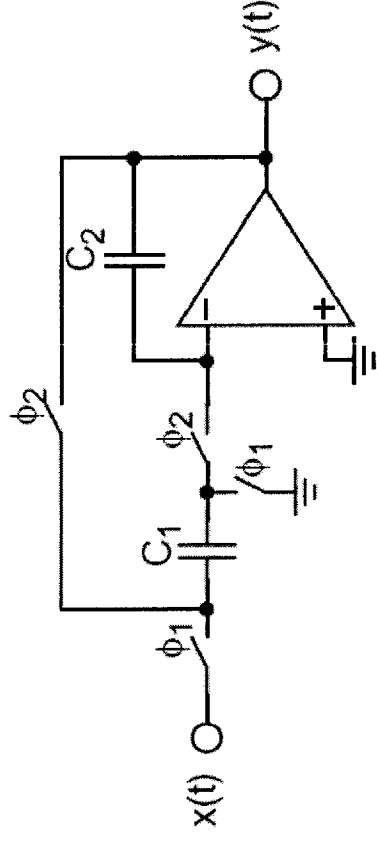
A 4th-order Bessel filter implemented with the inverse follow-the-leader topology.



Noise gains from each op-amp input



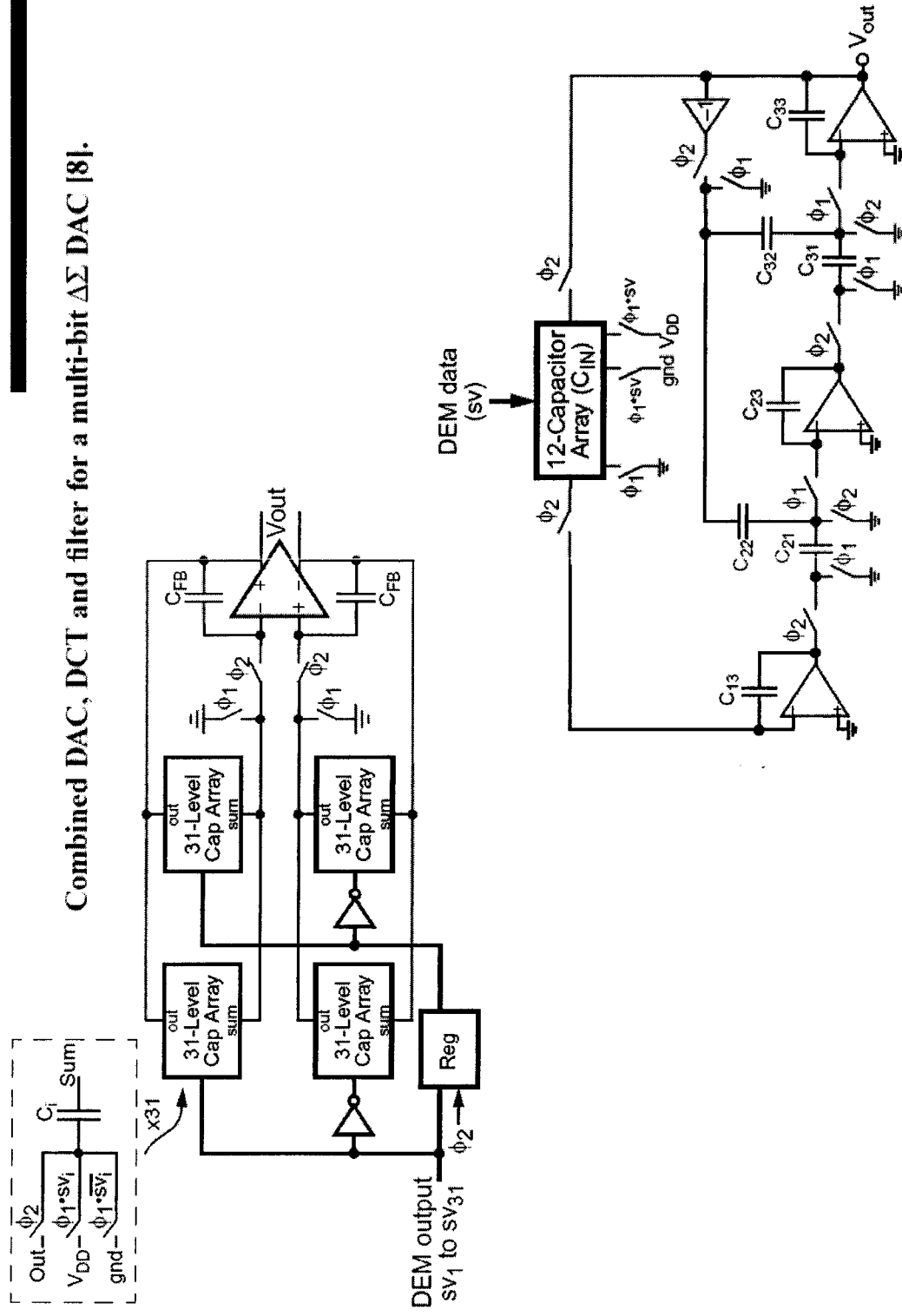
SC-CT BUFFER



A direct-charge-transfer (DCT) stage.

DESIGN EXAMPLES

Combined DAC, DCT and filter for a multi-bit $\Delta\Sigma$ DAC [8].



Another $\Delta\Sigma$ DAC with merged DAC, DCT and SCF filter functions [15].

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