12-Bit, 125 MSPS High Performance TxDAC® D/A Converter

AD9752*

FEATURES

High Performance Member of Pin-Compatible TxDAC Product Family
125 MSPS Update Rate
12-Bit Resolution
Excellent Spurious Free Dynamic Range Performance
SFDR to Nyquist @ 5 MHz Output: 79 dBc
Differential Current Outputs: 2 mA to 20 mA
Power Dissipation: 185 mW @ 5 V
Power-Down Mode: 20 mW @ 5 V
On-Chip 1.20 V Reference
CMOS-Compatible +2.7 V to +5.5 V Digital Interface
Package: 28-Lead SOIC and TSSOP
Edge-Triggered Latches

APPLICATIONS

Wideband Communication Transmit Channel:
Direct IF
Basestations
Wireless Local Loop
Digital Radio Link
Direct Digital Synthesis (DDS)
Instrumentation

PRODUCT DESCRIPTION

The AD9752 is a 12-bit resolution, wideband, second generation member of the TxDAC series of high performance, low power CMOS digital-to-analog-converters (DACs). The TxDAC family, which consists of pin compatible 8-, 10-, 12-, and 14-bit DACs, is specifically optimized for the transmit signal path of communication systems. All of the devices share the same interface options, small outline package and pinout, thus providing an upward or downward component selection path based on performance, resolution and cost. The AD9752 offers exceptional ac and dc performance while supporting update rates up to 125 MSPS.

The AD9752's flexible single-supply operating range of 4.5 V to 5.5 V and low power dissipation are well suited for portable and low power applications. Its power dissipation can be further reduced to a mere 65 mW, without a significant degradation in performance, by lowering the full-scale current output. Also, a power-down mode reduces the standby power dissipation to approximately 20 mW.

The AD9752 is manufactured on an advanced CMOS process. A segmented current source architecture is combined with a proprietary switching technique to reduce spurious components and enhance dynamic performance. Edge-triggered input latches and a 1.2 V temperature compensated bandgap reference have been integrated to provide a complete monolithic DAC solution. The digital inputs support +2.7 V to +5 V CMOS logic families.

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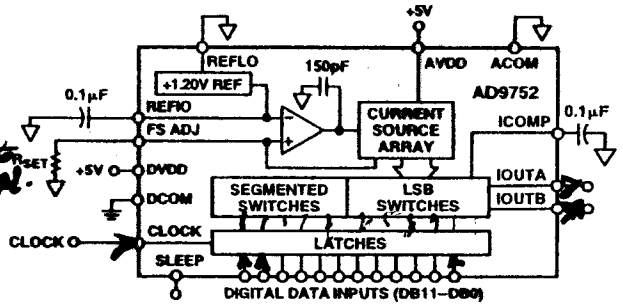
FUNCTIONAL BLOCK DIAGRAM



The AD9752 is a current-output DAC with a nominal full-scale output current of 20 mA and > 100 kΩ output impedance.

Differential current outputs are provided to support single-ended or differential applications. Matching between the two current outputs ensures enhanced dynamic performance in a differential output configuration. The current outputs may be tied directly to an output resistor to provide two complementary, single-ended voltage outputs or fed directly into a transformer. The output voltage compliance range is 1.25 V.

The on-chip reference and control amplifier are configured for maximum accuracy and flexibility. The AD9752 can be driven by the on-chip reference or by a variety of external reference voltages. The internal control amplifier, which provides a wide (>10:1) adjustment span, allows the AD9752 full-scale current to be adjusted over a 2 mA to 20 mA range while maintaining excellent dynamic performance. Thus, the AD9752 may operate at reduced power levels or be adjusted over a 20 dB range to provide additional gain ranging capabilities.

The AD9752 is available in 28-lead SOIC and TSSOP packages. It is specified for operation over the industrial temperature range.

PRODUCT HIGHLIGHTS

1. The AD9752 is a member of the wideband TxDAC product family that provides an upward or downward component selection path based on resolution (8 to 14 bits), performance and cost. The entire family of TxDACs is available in industry standard pinouts.
2. Manufactured on a CMOS process, the AD9752 uses a proprietary switching technique that enhances dynamic performance beyond that previously attainable by higher power/cost bipolar or BiCMOS devices.
3. On-chip, edge-triggered input CMOS latches interface readily to +2.7 V to +5 V CMOS logic families. The AD9752 can support update rates up to 125 MSPS.
4. A flexible single-supply operating range of 4.5 V to 5.5 V and a wide full-scale current adjustment span of 2 mA to 20 mA allow the AD9752 to operate at reduced power levels.
5. The current output(s) of the AD9752 can be easily configured for various single-ended or differential circuit topologies.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703
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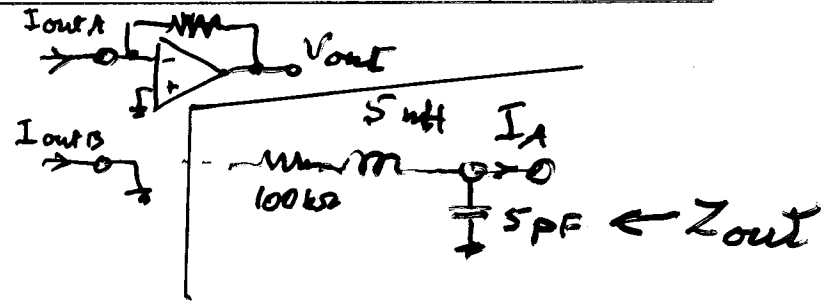
AD9752—SPECIFICATIONS

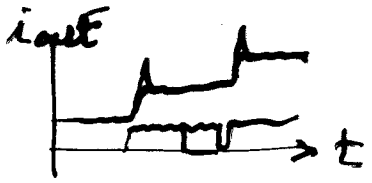
DC SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = +5 V, DVDD = +5 V, I_{OUTFS} = 20 mA, unless otherwise noted)

Parameter	Min	Typ	Max	Units
RESOLUTION	12			Bits
DC ACCURACY[1]				
Integral Linearity Error (INL)				
T_A = +25°C	–1.5	±0.5	+1.5	LSB
T_{MIN} to T_{MAX}	–2.0		+2.0	LSB
Differential Nonlinearity (DNL)				
T_A = +25°C	–0.75	±0.25	+0.75	LSB
T_{MIN} to T_{MAX}	–1.0		+1.0	LSB
ANALOG OUTPUT				
Offset Error	–0.02		+0.02	% of FSR
Gain Error (Without Internal Reference)	–2	±0.5	+2	% of FSR
Gain Error (With Internal Reference)	–5	±1.5	+5	% of FSR
Full-Scale Output Current[2]	2.0		20.0	mA
Output Compliance Range	–1.0		1.25	V
Output Resistance		100		kΩ
Output Capacitance		5		pF
REFERENCE OUTPUT				
Reference Voltage	1.14	1.20	1.26	V
Reference Output Current[3]		100		nA
REFERENCE INPUT				
Input Compliance Range	0.1		1.25	V
Reference Input Resistance		1		MΩ
Small Signal Bandwidth		0.5		MHz
TEMPERATURE COEFFICIENTS				
Offset Drift		0		ppm of FSR/°C
Gain Drift (Without Internal Reference)		±50		ppm of FSR/°C
Gain Drift (With Internal Reference)		±100		ppm of FSR/°C
Reference Voltage Drift		±50		ppm/°C
POWER SUPPLY				
Supply Voltages				
AVDD	4.5	5.0	5.5	V
DVDD	2.7	5.0	5.5	V
Analog Supply Current (I_{AVDD})[4]		34	39	mA
Digital Supply Current (I_{DVDD})[5]		3	5	mA
Supply Current Sleep Mode (I_{AVDD})[6]		4	8	mA
Power Dissipation[5] (5 V, I_{OUTFS} = 20 mA)		185	220	mW
Power Supply Rejection Ratio[7]—AVDD	–0.4		+0.4	% of FSR/V
Power Supply Rejection Ratio[7]—DVDD	–0.025		+0.025	% of FSR/V
OPERATING RANGE	–40		+85	°C

NOTES
[1]Measured at IOUTA, driving a virtual ground.
[2]Nominal full-scale current, I_{OUTFS}, is 32 × the I_{REF} current.
[3]Use an external buffer amplifier to drive any external load.
[4]Requires +5 V supply.
[5]Measured at f_{CLOCK} = 25 MSPS and I_{OUT} = static full scale (20 mA).
[6]Logic level for SLEEP pin must be referenced to AVDD. Min V_{IH} = 3.5 V.
[7]±5% Power supply variation.

Specifications subject to change without notice.





DYNAMIC SPECIFICATIONS

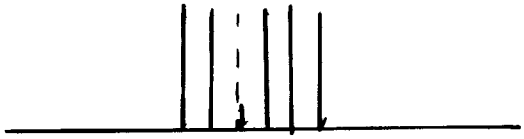
(T_{MIN} to T_{MAX}, AVDD = +5 V, BVDD = +5 V, I_{OUTFS} = 20 mA, Differential Transformer Coupled Output, 50 Ω Doubly Terminated, unless otherwise noted)

Parameter	Min	Typ	Max	Units
DYNAMIC PERFORMANCE				
Maximum Output Update Rate (f_{CLOCK})	125			MSPS
Output Settling Time (t_{ST}) (to 0.1%)[1]		35		ns
Output Propagation Delay (t_{PD})		1		ns
Glitch Impulse		5		pV-s
Output Rise Time (10% to 90%)[1]		2.5		ns
Output Fall Time (10% to 90%)[1]		2.5		ns
Output Noise (I_{OUTFS} = 20 mA)		50		pA/√Hz
Output Noise (I_{OUTFS} = 2 mA)		30		pA/√Hz
AC LINEARITY				
Spurious-Free Dynamic Range to Nyquist				
f_{CLOCK} = 25 MSPS; f_{OUT} = 1.00 MHz				
0 dBFS Output				
T_A = +25°C		84		dBc
−6 dBFS Output		76		dBc
−12 dBFS Output		81		dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 1.00 MHz		81		dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 2.51 MHz		81		dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 5.02 MHz		76		dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 14.02 MHz		62		dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 20.2 MHz		60		dBc
f_{CLOCK} = 100 MSPS; f_{OUT} = 2.5 MHz		78		dBc
f_{CLOCK} = 100 MSPS; f_{OUT} = 5 MHz		76		dBc
f_{CLOCK} = 100 MSPS; f_{OUT} = 20 MHz		63		dBc
f_{CLOCK} = 100 MSPS; f_{OUT} = 40 MHz		55		dBc
Spurious-Free Dynamic Range within a Window				
f_{CLOCK} = 25 MSPS; f_{OUT} = 1.00 MHz	84	93		dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 5.02 MHz; 2 MHz Span		86		dBc
f_{CLOCK} = 100 MSPS; f_{OUT} = 5.04 MHz; 4 MHz Span		86		dBc
Total Harmonic Distortion				
f_{CLOCK} = 25 MSPS; f_{OUT} = 1.00 MHz				
T_A = +25°C		−82	−74	dBc
f_{CLOCK} = 50 MHz; f_{OUT} = 2.00 MHz		−76		dBc
f_{CLOCK} = 100 MHz; f_{OUT} = 2.00 MHz		−76		dBc
Multitone Power Ratio (8 Tones at 110 kHz Spacing)				
f_{CLOCK} = 20 MSPS; f_{OUT} = 2.00 MHz to 2.99 MHz				
0 dBFS Output		81		dBc
−6 dBFS Output		81		dBc
−12 dBFS Output		85		dBc
−18 dBFS Output		86		dBc

NOTES

[1]Measured single ended into 50 Ω load.

Specifications subject to change without notice.



DEFINITIONS OF SPECIFICATIONS

Linearity Error (Also Called Integral Nonlinearity or INL)
Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (or DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A D/A converter is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
The deviation of the output current from the ideal of zero is called offset error. For IOUTA, 0 mA output is expected when the inputs are all 0s. For IOUTB, 0 mA output is expected when all inputs are set to 1s.

Gain Error
The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1s minus the output when all inputs are set to 0s.

Output Compliance Range
The range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (+25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per °C. For reference drift, the drift is reported in ppm per °C.

Power Supply Rejection
The maximum change in the full-scale output as the supplies are varied from nominal to minimum and maximum specified voltages.

Settling Time
The time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

Glitch Impulse
Asymmetrical switching times in a DAC give rise to undesired output transients that are quantified by a glitch impulse. It is specified as the net area of the glitch in pV-s.

Spurious-Free Dynamic Range
The difference, in dB, between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Total Harmonic Distortion
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal. It is expressed as a percentage or in decibels (dB).

Multitone Power Ratio
The spurious-free dynamic range for an output containing multiple carrier tones of equal amplitude. It is measured as the difference between the rms amplitude of a carrier tone to the peak spurious signal in the region of a removed tone.

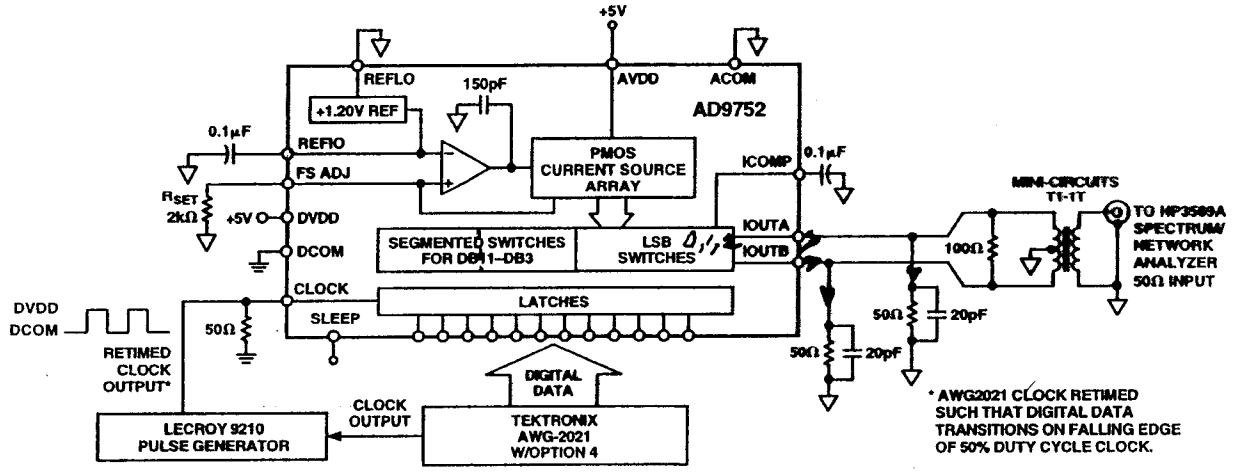
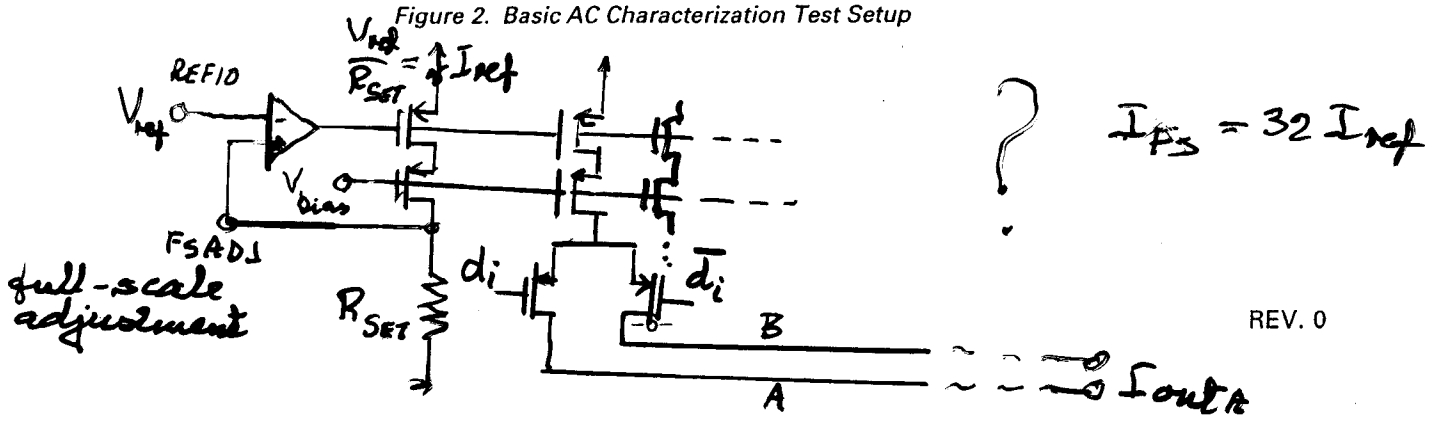


Figure 2. Basic AC Characterization Test Setup



Typical AC Characterization Curves @ +5 V Supplies

(AVDD = +5 V, DVDD = +5 V, I_{OUTFS} = 20 mA, 50 Ω Doubly Terminated Load, Differential Output, T_A = +25°C, SFDR up to Nyquist, unless otherwise noted)

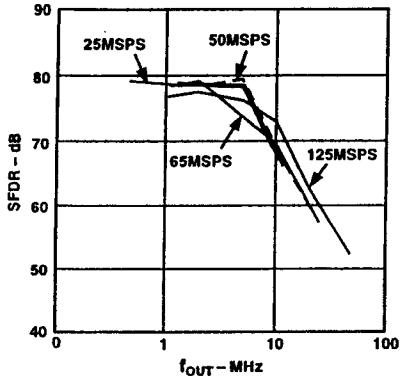


Figure 3. SFDR vs. f_{OUT} @ 0 dBFS

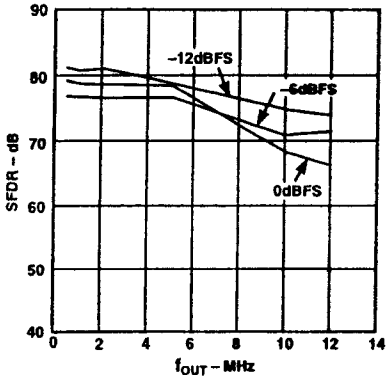


Figure 4. SFDR vs. f_{OUT} @ 25 MSPS

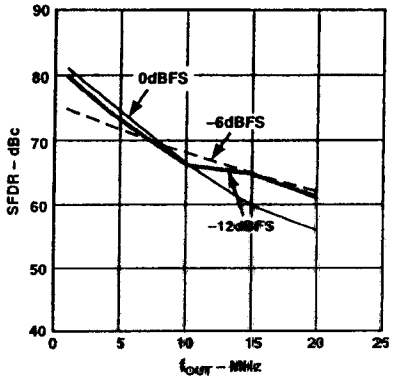


Figure 5. SFDR vs. f_{OUT} @ 50 MSPS

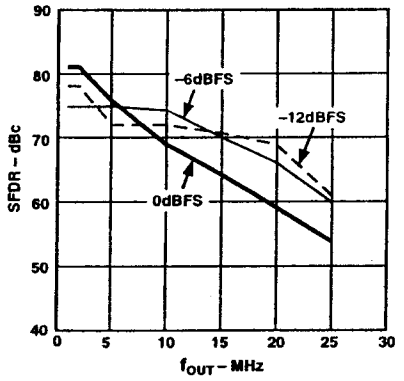


Figure 6. SFDR vs. f_{OUT} @ 65 MSPS

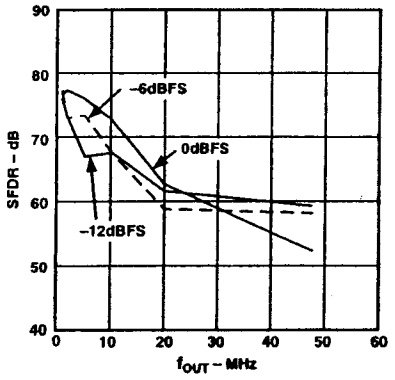


Figure 7. SFDR vs. f_{OUT} @ 125 MSPS

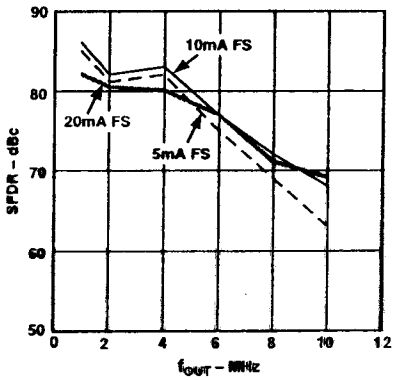


Figure 8. SFDR vs. f_{OUT} and I_{OUTFS} @ 25 MSPS and 0 dBFS

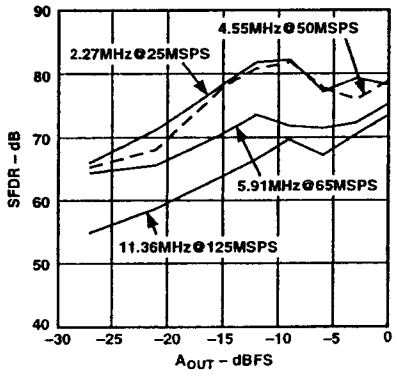


Figure 9. Single-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLOCK}/11$

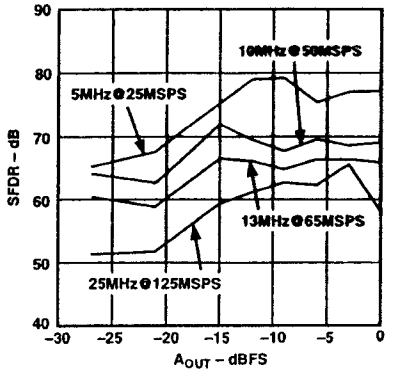


Figure 10. Single-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLOCK}/5$

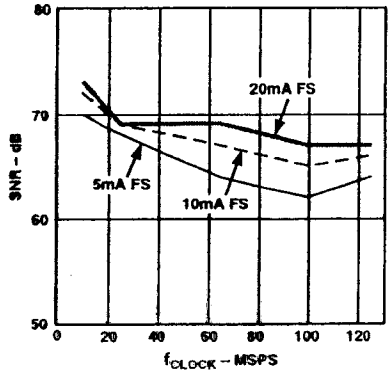


Figure 11. SNR vs. f_{CLOCK} and I_{OUTFS} @ f_{OUT} = 2 MHz and 0 dBFS

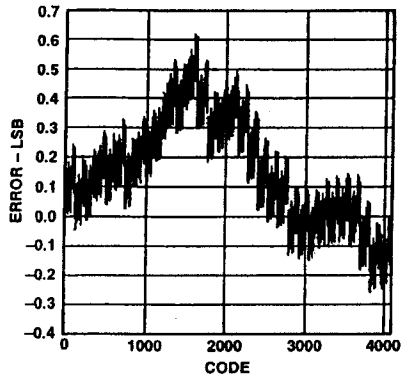


Figure 12. Typical INL

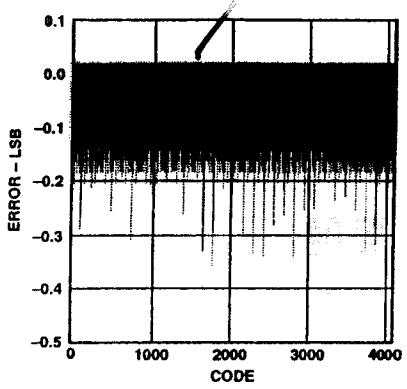


Figure 13. Typical DNL

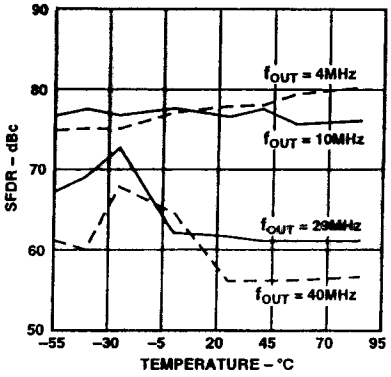


Figure 14. SFDR vs. Temperature @ 125 MSPS, 0 dBFS

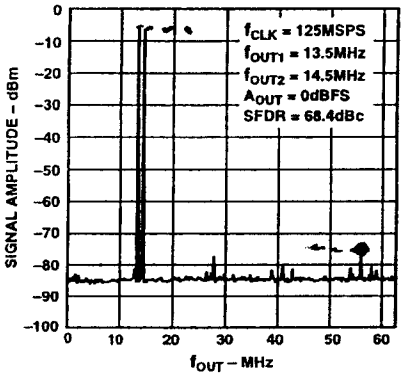


Figure 15. Dual-Tone SFDR

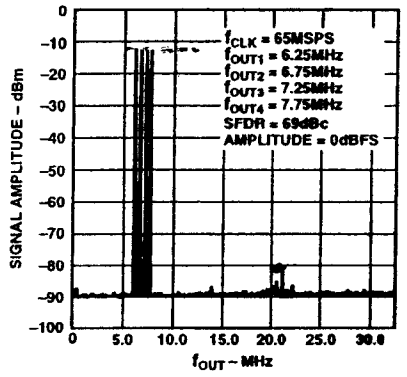
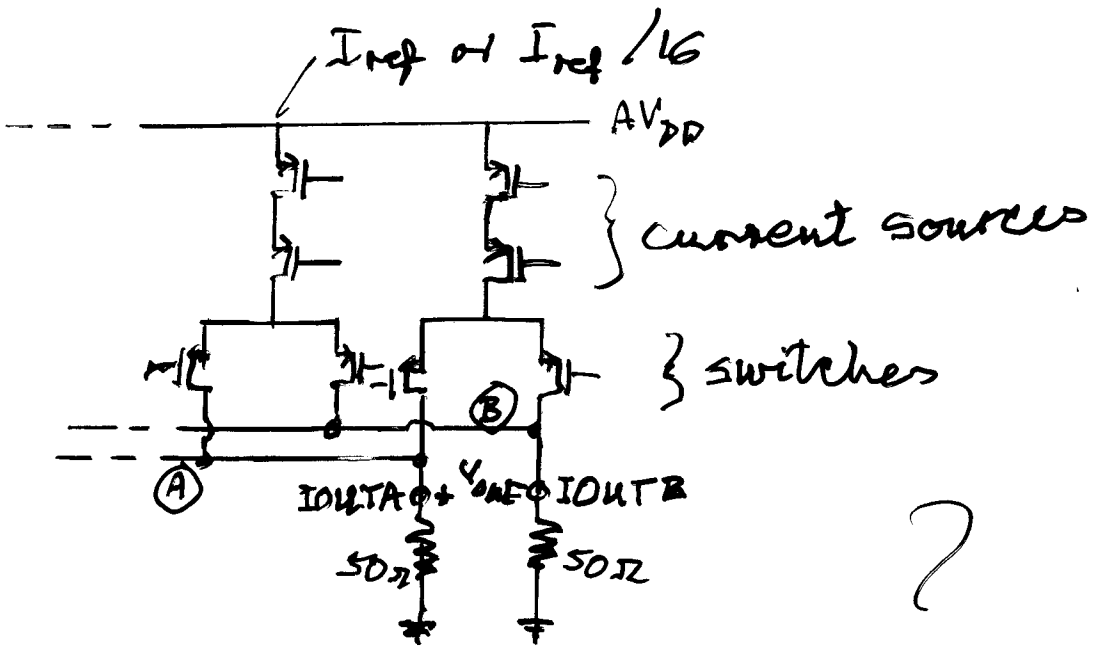


Figure 16. Four-Tone SFDR



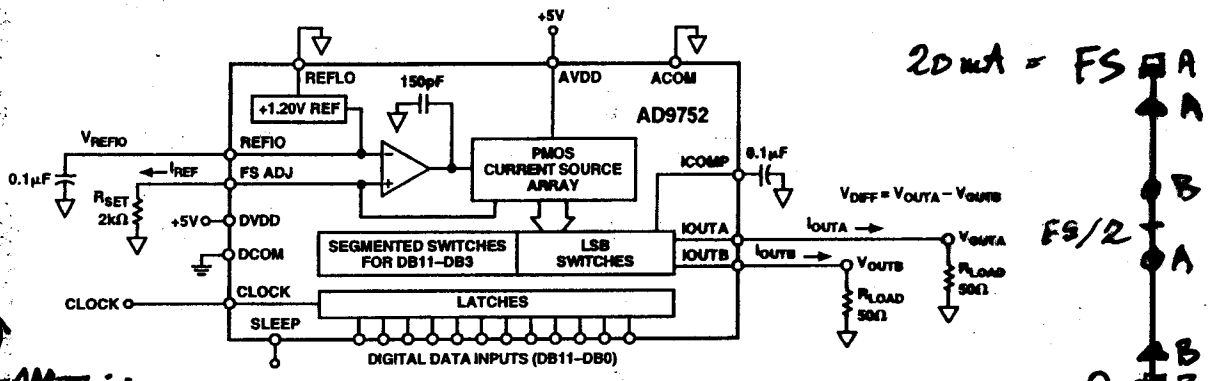


Figure 17. Functional Block Diagram

FUNCTIONAL DESCRIPTION

Figure 17 shows a simplified block diagram of the AD9752. The AD9752 consists of a large PMOS current source array that is capable of providing up to 20 mA of total current. The array is divided into 31 equal currents that make up the five most significant bits (MSBs). The next four bits or middle bits consist of 15 equal current sources whose value is 1/16th of an MSB current source. The remaining LSBs are binary weighted fractions of the middle-bits current sources. Implementing the middle and lower bits with current sources, instead of an R-2R ladder, enhances its dynamic performance for multitone or low amplitude signals and helps maintain the DAC's high output impedance (i.e., >100 kΩ).

All of these current sources are switched to one or the other of the two output nodes (i.e., IOUTA or IOUTB) via PMOS differential current switches. The switches are based on a new architecture that drastically improves distortion performance. This new switch architecture reduces various timing errors and provides matching complementary drive signals to the inputs of the differential current switches.

The analog and digital sections of the AD9752 have separate power supply inputs (i.e., AVDD and DVDD). The digital section, which is capable of operating up to a 125 MSPS clock rate and over a +2.7 V to +5.5 V operating range, consists of edge-triggered latches and segment decoding logic circuitry. The analog section, which can operate over a +4.5 V to +5.5 V range, includes the PMOS current sources, the associated differential switches, a 1.20 V bandgap voltage reference and a reference control amplifier.

The full-scale output current is regulated by the reference control amplifier and can be set from 2 mA to 20 mA via an external resistor, R_{SET}. The external resistor, in combination with both the reference control amplifier and voltage reference V_{REFIO}, sets the reference current I_{REF}, which is mirrored over to the segmented current sources with the proper scaling factor. The full-scale current, I_{OUTFS}, is thirty-two times the value of I_{REF}.

DAC TRANSFER FUNCTION

The AD9752 provides complementary current outputs, IOUTA and IOUTB. IOUTA will provide a near full-scale current output, I_{OUTFS}, when all bits are high (i.e., DAC CODE = 4095) while IOUTB, the complementary output, provides no current. The current output appearing at IOUTA and IOUTB is a function of both the input code and I_{OUTFS} and can be expressed as:

$$IOUTA = (DAC\ CODE/4096) \times I_{OUTFS} \quad (1)$$

$$IOUTB = (4095 - DAC\ CODE)/4096 \times I_{OUTFS} \quad (2)$$

where *DAC CODE* = 0 to 4095 (i.e., Decimal Representation).

As mentioned previously, I_{OUTFS} is a function of the reference current I_{REF}, which is nominally set by a reference voltage V_{REFIO} and external resistor R_{SET}. It can be expressed as:

$$I_{OUTFS} = 32 \times I_{REF} \quad (3)$$

where $I_{REF} = V_{REFIO}/R_{SET}$ (4)

The two current outputs will typically drive a resistive load directly or via a transformer. If dc coupling is required, IOUTA and IOUTB should be directly connected to matching resistive loads, R_{LOAD}, which are tied to analog common, ACOM. Note, R_{LOAD} may represent the equivalent load resistance seen by IOUTA or IOUTB as would be the case in a doubly terminated 50 Ω or 75 Ω cable. The single-ended voltage output appearing at the IOUTA and IOUTB nodes is simply :

$$V_{OUTA} = IOUTA \times R_{LOAD} \quad (5)$$

$$V_{OUTB} = IOUTB \times R_{LOAD} \quad (6)$$

Note the full-scale value of V_{OUTA} and V_{OUTB} should not exceed the specified output compliance range to maintain specified distortion and linearity performance.

The differential voltage, V_{DIFF}, appearing across IOUTA and IOUTB is:

$$V_{DIFF} = (IOUTA - IOUTB) \times R_{LOAD} \quad (7)$$

Substituting the values of I_{OUTA}, I_{OUTB}, and I_{REF}; V_{DIFF} can be expressed as:

$$V_{DIFF} = \{(2\ DAC\ CODE - 4095)/4096\} \times (32\ R_{LOAD}/R_{SET}) \times V_{REFIO} \quad (8)$$

These last two equations highlight some of the advantages of operating the AD9752 differentially. First, the differential operation will help cancel common-mode error sources associated with I_{OUTA} and I_{OUTB} such as noise, distortion and dc offsets. Second, the differential code dependent current and subsequent voltage, V_{DIFF}, is twice the value of the single-ended voltage output (i.e., V_{OUTA} or V_{OUTB}), thus providing twice the signal power to the load.

Note, the gain drift temperature performance for a single-ended (V_{OUTA} and V_{OUTB}) or differential output (V_{DIFF}) of the AD9752 can be enhanced by selecting temperature tracking resistors for R_{LOAD} and R_{SET} due to their ratiometric relationship as shown in Equation 8.

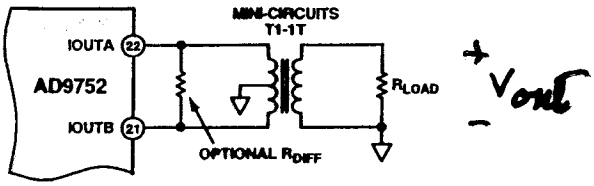


Figure 28. Differential Output Using a Transformer

The center tap on the primary side of the transformer must be connected to ACOM to provide the necessary dc current path for both IOUTA and IOUTB. The complementary voltages appearing at IOUTA and IOUTB (i.e., V_{OUTA} and V_{OUTB}) swing symmetrically around ACOM and should be maintained with the specified output compliance range of the AD9752. A differential resistor, R_{DIFF}, may be inserted in applications in which the output of the transformer is connected to the load, R_{LOAD}, via a passive reconstruction filter or cable. R_{DIFF} is determined by the transformer's impedance ratio and provides the proper source termination which results in a low VSWR. Note that approximately half the signal power will be dissipated across R_{DIFF}.

DIFFERENTIAL USING AN OP AMP

An op amp can also be used to perform a differential to single-ended conversion as shown in Figure 29. The AD9752 is configured with two equal load resistors, R_{LOAD}, of 25 Ω. The differential voltage developed across IOUTA and IOUTB is converted to a single-ended signal via the differential op amp configuration. An optional capacitor can be installed across IOUTA and IOUTB forming a real pole in a low-pass filter. The addition of this capacitor also enhances the op amps distortion performance by preventing the DACs high slewing output from overloading the op amp's input.

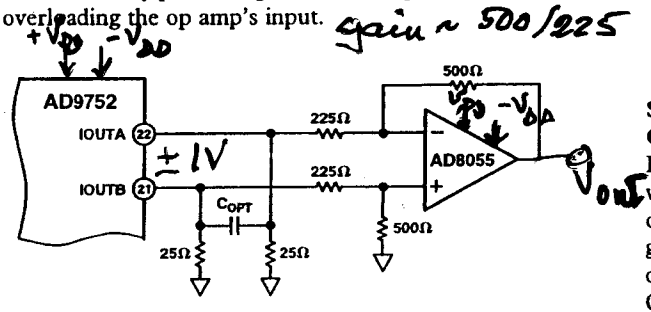


Figure 29. DC Differential Coupling Using an Op Amp

The common-mode rejection of this configuration is typically determined by the resistor matching. In this circuit, the differential op amp circuit is configured to provide some additional signal gain. The op amp must operate off of a dual supply since its output is approximately ±1.0 V. A high speed amplifier such as the AD8055 or AD9632 capable of preserving the differential performance of the AD9752 while meeting other system level objectives (i.e., cost, power) should be selected. The op amps differential gain, its gain setting resistor values, and full-scale output swing capabilities should all be considered when optimizing this circuit.

The differential circuit shown in Figure 30 provides the necessary level-shifting required in a single supply system. In this case, AVDD which is the positive analog supply for both the AD9752 and the op amp is also used to level-shift the differential output of the AD9752 to midsupply (i.e., AVDD/2). The AD8041 is a suitable op amp for this application.

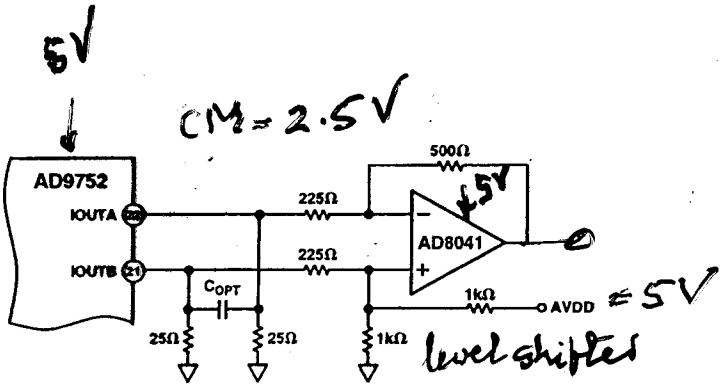


Figure 30. Single-Supply DC Differential Coupled Circuit

SINGLE-ENDED UNBUFFERED VOLTAGE OUTPUT

Figure 31 shows the AD9752 configured to provide a unipolar output range of approximately 0 V to +0.5 V for a doubly terminated 50 Ω cable since the nominal full-scale current, I_{OUTFS}, of 20 mA flows through the equivalent R_{LOAD} of 25 Ω. In this case, R_{LOAD} represents the equivalent load resistance seen by IOUTA or IOUTB. The unused output (IOUTA or IOUTB) can be connected to ACOM directly or via a matching R_{LOAD}. Different values of I_{OUTFS} and R_{LOAD} can be selected as long as the positive compliance range is adhered to. One additional consideration in this mode is the integral nonlinearity (INL) as discussed in the ANALOG OUTPUT section of this data sheet. For optimum INL performance, the single-ended, buffered voltage output configuration is suggested.

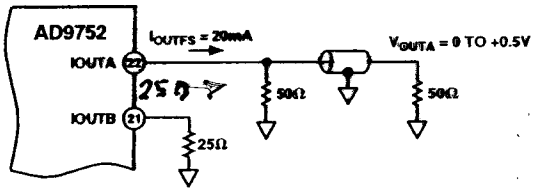


Figure 31. 0 V to +0.5 V Unbuffered Voltage Output

SINGLE-ENDED, BUFFERED VOLTAGE OUTPUT CONFIGURATION

Figure 32 shows a buffered single-ended output configuration in which the op amp U1 performs an I-V conversion on the AD9752 output current. U1 maintains IOUTA (or IOUTB) at a virtual ground, thus minimizing the nonlinear output impedance effect on the DAC's INL performance as discussed in the ANALOG OUTPUT section. Although this single-ended configuration typically provides the best dc linearity performance, its ac distortion performance at higher DAC update rates may be limited by U1's slewing capabilities. U1 provides a negative unipolar output voltage and its full-scale output voltage is simply the product of R_{FB} and I_{OUTFS}. The full-scale output should be set within U1's voltage output swing capabilities by scaling I_{OUTFS} and/or R_{FB}. An improvement in ac distortion performance may result with a reduced I_{OUTFS} since the signal current U1 will be required to sink will be subsequently reduced.

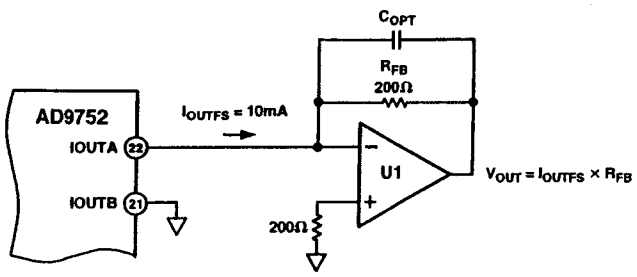


Figure 32. Unipolar Buffered Voltage Output

POWER AND GROUNDING CONSIDERATIONS, POWER SUPPLY REJECTION

Many applications seek high speed and high performance under less than ideal operating conditions. In these circuits, the implementation and construction of the printed circuit board design is as important as the circuit design. Proper RF techniques must be used for device selection, placement and routing as well as power supply bypassing and grounding to ensure optimum performance. Figures 42-47 illustrate the recommended printed circuit board ground, power and signal plane layouts which are implemented on the AD9752 evaluation board.

One factor that can measurably affect system performance is the ability of the DAC output to reject dc variations or ac noise superimposed on the analog or digital dc power distribution (i.e., AVDD, DVDD). This is referred to as Power Supply Rejection Ratio (PSRR). For dc variations of the power supply, the resulting performance of the DAC directly corresponds to a gain error associated with the DAC's full-scale current, I_{OUTFS}. AC noise on the dc supplies is common in applications where the power distribution is generated by a switching power supply. Typically, switching power supply noise will occur over the spectrum from tens of kHz to several MHz. PSRR vs. frequency of the AD9752 AVDD supply, over this frequency range, is given in Figure 33.

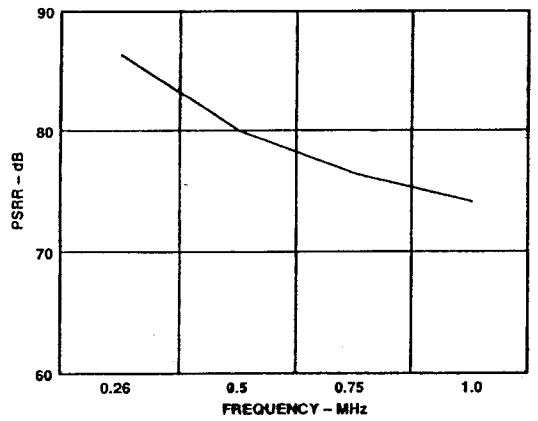


Figure 33. Power Supply Rejection Ratio of AD9752

Note that the units in Figure 33 are given in units of (amps out)/(volts in). Noise on the analog power supply has the effect of modulating the internal switches, and therefore the output current. The voltage noise on the dc power, therefore, will be added in a nonlinear manner to the desired I_{OUT}. Due to the relative different sizes of these switches, PSRR is very code dependent. This can produce a mixing effect which can modulate low frequency power supply noise to higher frequencies. Worst case PSRR for either one of the differential DAC outputs will occur when the full-scale current is directed towards that output. As a result, the PSRR measurement in Figure 33 represents a worst case condition in which the digital inputs remain static and the full scale output current of 20 mA is directed to the DAC output being measured.

An example serves to illustrate the effect of supply noise on the analog supply. Suppose a switching regulator with a switching frequency of 250 kHz produces 10 mV rms of noise and for simplicity sake (i.e., ignore harmonics), all of this noise is concentrated at 250 kHz. To calculate how much of this undesired noise will appear as current noise super imposed on the DAC's full-scale current, I_{OUTFS}, one must determine the PSRR in dB using Figure 33 at 250 kHz. To calculate the PSRR for a given R_{LOAD}, such that the units of PSRR are converted from A/V to V/V, adjust the curve in Figure 33 by the scaling factor 20 × Log (R_{LOAD}). For instance, if R_{LOAD} is 50 Ω, the PSRR is reduced by 34 dB (i.e., PSRR of the DAC at 1 MHz which is 74 dB in Figure 33 becomes 40 dB V_{OUT}/V_{IN}).

Proper grounding and decoupling should be a primary objective in any high speed, high resolution system. The AD9752 features separate analog and digital supply and ground pins to optimize the management of analog and digital ground currents in a system. In general, AVDD, the analog supply, should be decoupled to ACOM, the analog common, as close to the chip as physically possible. Similarly, DVDD, the digital supply, should be decoupled to DCOM as close as physically as possible.

For those applications that require a single +5 V or +3 V supply for both the analog and digital supply, a clean analog supply may be generated using the circuit shown in Figure 34. The circuit consists of a differential LC filter with separate power supply and return lines. Lower noise can be attained using low ESR type electrolytic and tantalum capacitors.

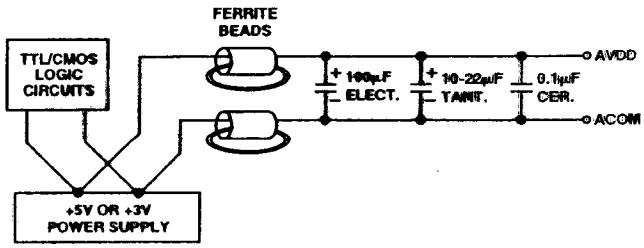


Figure 34. Differential LC Filter for Single +5 V or +3 V Applications

Maintaining low noise on power supplies and ground is critical to obtaining optimum results from the AD9752. If properly implemented, ground planes can perform a host of functions on high speed circuit boards: bypassing, shielding, current transport, etc. In mixed signal design, the analog and digital portions of the board should be distinct from each other, with the analog ground plane confined to the areas covering the analog signal traces, and the digital ground plane confined to areas covering the digital interconnects.

All analog ground pins of the DAC, reference and other analog components should be tied directly to the analog ground plane. The two ground planes should be connected by a path 1/8 to 1/4 inch wide underneath or within 1/2 inch of the DAC to