

Slide Set

Data Converters

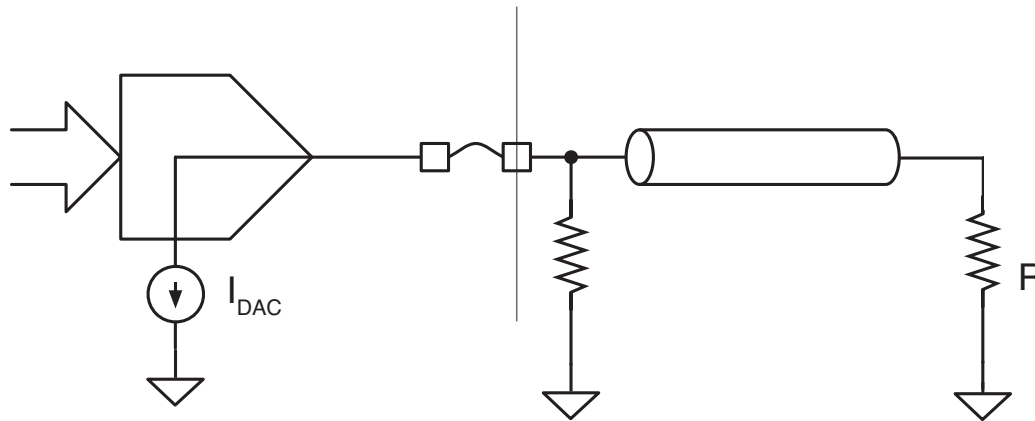
Nyquist-rate D/A Converters

Summary

- Introduction
- Types of Converters
- Resistor-based Architectures
- Capacitor-based Architectures
- Current Source-based Architectures
- Other Architectures

Introduction

The input of a *DAC* is a multi-bit digital signal while the output is a voltage or a current capable of driving an external load.



Often the current is used to drive an off-chip coaxial cable to yield a voltage across the terminations.

Introduction (ii)

Many *DACs* use integrated resistances or capacitors to attenuate (or amplify) the reference.

A careful design of the layout leads to matching accuracies in the order of 0.02 – 0.1 %. Thus, resolutions and linearity of up to 60 – 70 *dB* are possible without trimming of analog passive elements and without using digital correction or digital calibration.

Use of analog *CMOS* switches: low on-resistance, high speed of switching and minimum side effects.

Use of clock booster.

Control of the *clock-feedthrough*

DAC Applications

DAC for video:

HDTV monitor displays more than 1000 lines per frame. In addition to the higher resolution a *HDTV* monitor also provides a higher contrast ratio and a more detailed color range. To maximize the viewing quality on a state-of-art display technology, 12-bit and 150 *MSPS* conversion rate are therefore often necessary.

DACs for wired and wireless communications:

DACs for *ADSL* or *ADLS2+* must handle signal bands of 1.1 *MHz* or 2.2 *MHz* with 12-bit of resolution.

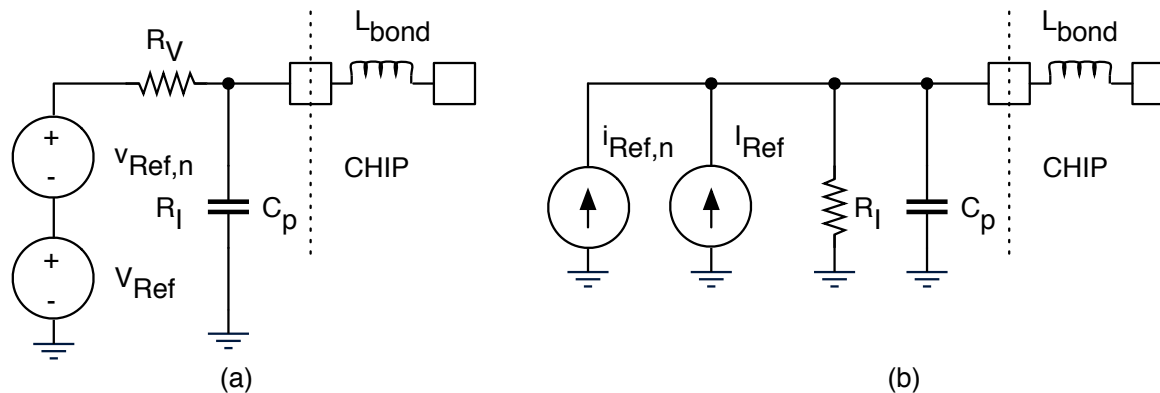
UMTS, *CDMA2000*, and *GSM/EDGE* require both high conversion rates and high resolution especially when multiple carriers are used instead of a single signal generating source. Conversion rates of 200 *MSPS* - 1 *GSpS* and resolutions from 12-bit to 16-bit can be necessary.

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Voltage and Current References

Voltage or current references can be either generated inside the chip or provided via an external pin.



Noise spectral level must be well below the quantization floor

$$v_{Ref,n}^2 \ll \frac{V_{FS}^2}{6 \cdot 2^{2n} \cdot f_s} \quad \text{or} \quad i_{Ref,n}^2 \ll \frac{I_{FS}^2}{6 \cdot 2^{2n} \cdot f_s}. \quad (1)$$

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The reference issue requires always to ...

Remember

The noise of reference generators must be lower than the expected quantization noise floor. The request becomes very challenging for resolutions above 14-bit.

Remind that the spectrum of the input referred noise generator of an *MOS* transistor is $v_n^2 = (8/3)kT/g_m$. Just a single *MOS* transistor which transconductance is equal to 0.2 mA/V gives to a noise spectrum as large as $v_n^2 = 7.4 \text{ nV} \sqrt{\text{Hz}}$

Types of Converters

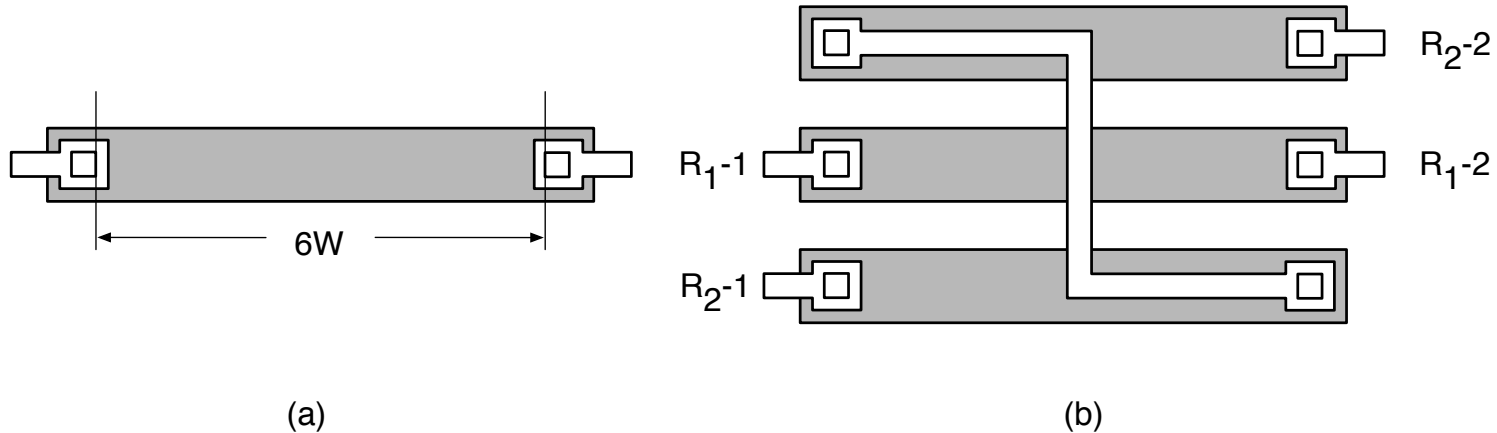
The basic components used in a *DAC* architecture normally classify the *DAC*. We distinguish between:

- Resistor based architectures.
- Capacitor based architectures.
- Current source based architectures.

Resistor based Architectures

Strips of resistive layers with a given specific resistance, ρ_{\square} . The effective number of squares $(L/W)_{eff}$ and the contact resistance R_{cont} give the total resistive value

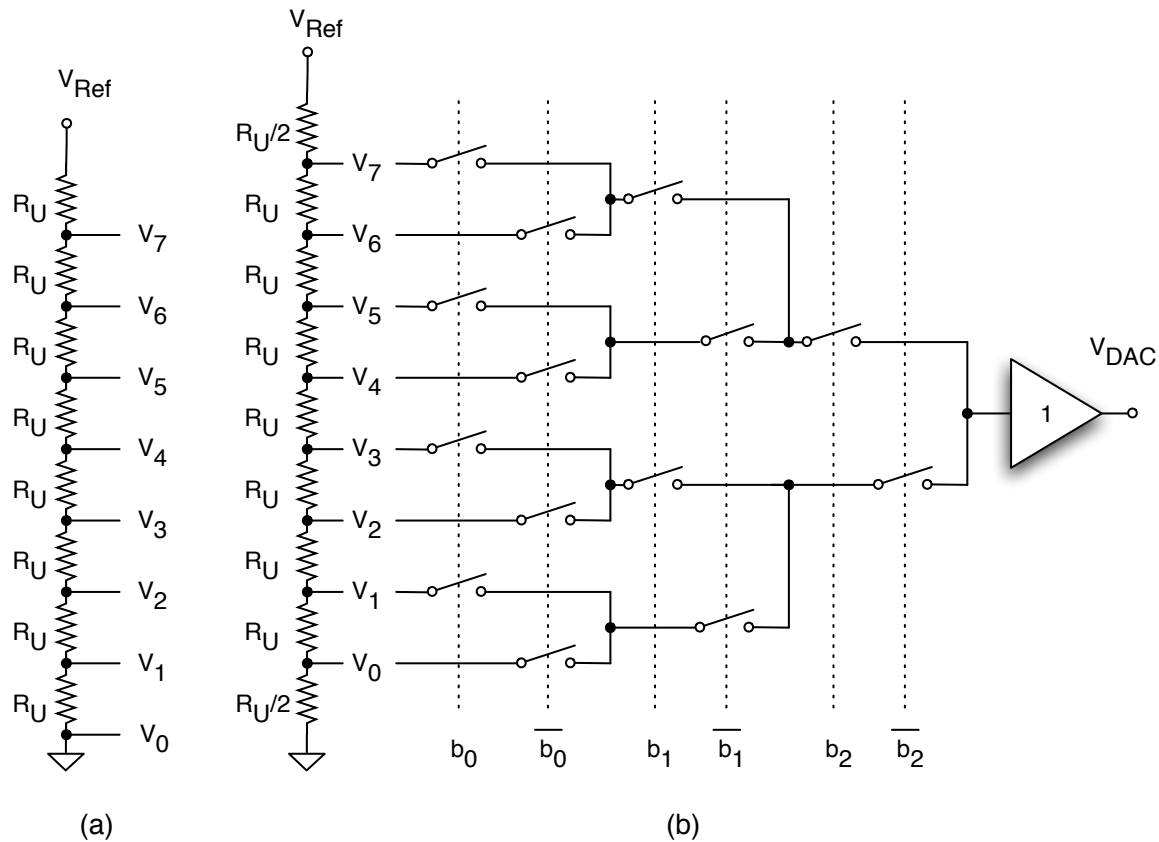
$$R = \rho_{\square}(L/W)_{eff} + 2 \cdot R_{cont}. \quad (2)$$



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Resistive Divider

Kelvin divider invented by Lord Kelvin in the 18th century.



Resistive Divider (cont.)

2^3 equal resistors, R_U , generate 8 discrete analog voltages

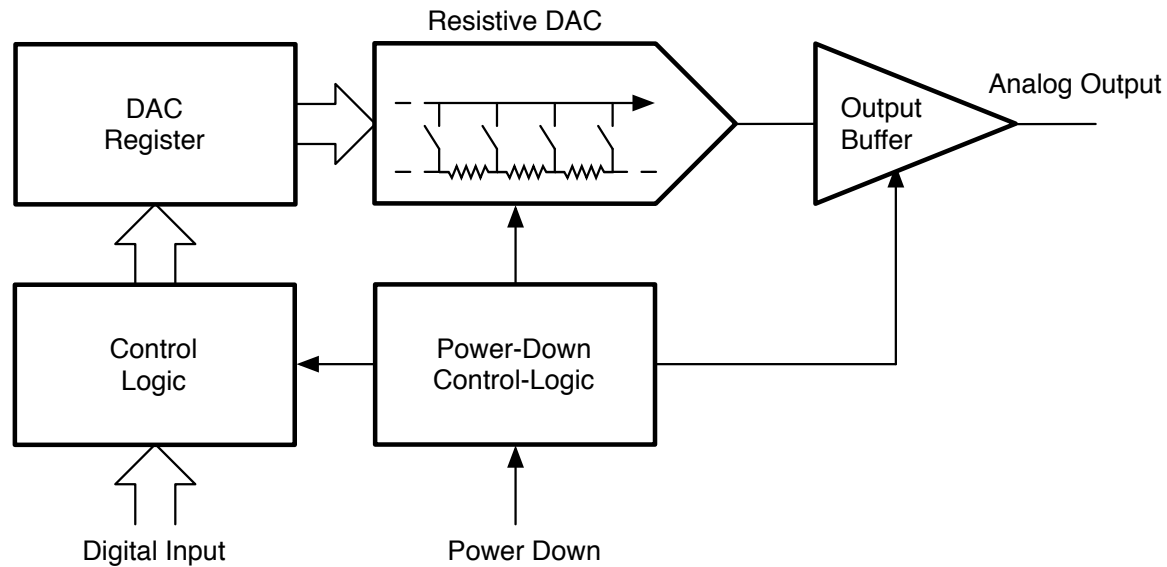
$$V_i = V_{Ref} \frac{i}{8} \quad i = 0 \dots 7. \quad (3)$$

The resistive divider (b) shifts the voltages by half an *LSB* ($V_{Ref}/2^{n+1}$) by moving a half unity resistance, $R_U/2$, from the top to the bottom of the resistive divider.

The selection of a voltage is done by a tree of switches whose *on* or *off* condition is controlled by the digital input.

The buffer provides a very high input impedance so as performing a volt-metric measurement). The buffer also provides a low output impedance for properly driving the *DAC* load.

Unary Selection



Only one switch on the Kelvin divider-buffer path but many control lines

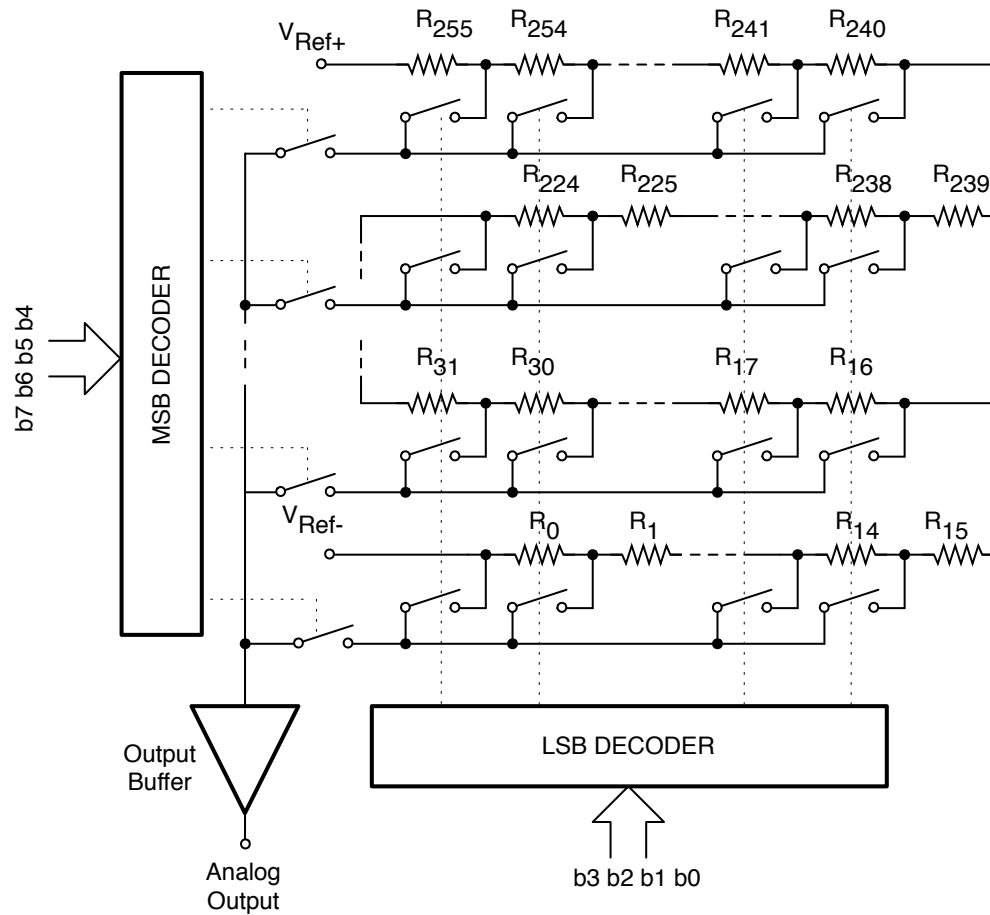
For decoding the digital input there is a ...

Trade-off

The decoding method used to select the Kelvin divider voltages depends on a trade-off between speed, complexity, and power consumption.

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X-Y Selection



Settling of the Output Voltage

Assume that the speed of the buffer is very large \rightarrow the voltage at the input and output of the buffer depends on an RC response

$$R_{eq} = \frac{(k-1)(2^n - k + 1)}{2^n} R_U + N_{on} \cdot R_{on}. \quad (4)$$

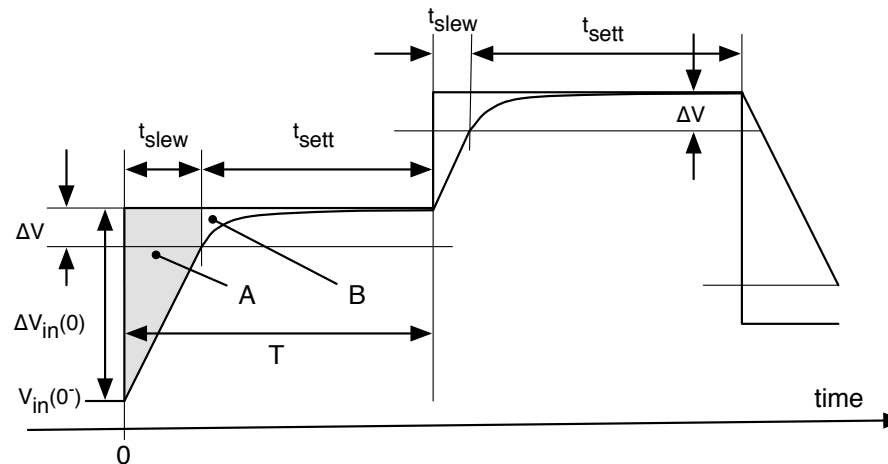
$$C_{in} = C_{in,B} + N_{on} \cdot C_{p,on} + N_{off} \cdot C_{p,off}, \quad (5)$$

$C_{in,B}$ is the input capacitance of the buffer; N_{on} and N_{off} on and off switches; and $C_{p,on} \simeq C_{p,off}$ are parasitic capacitances.

C_{in} almost constant. R_{eq} depends on the selected tap

non-linear time-constant!

If the slew-rate and bandwidth of the buffer matter ...



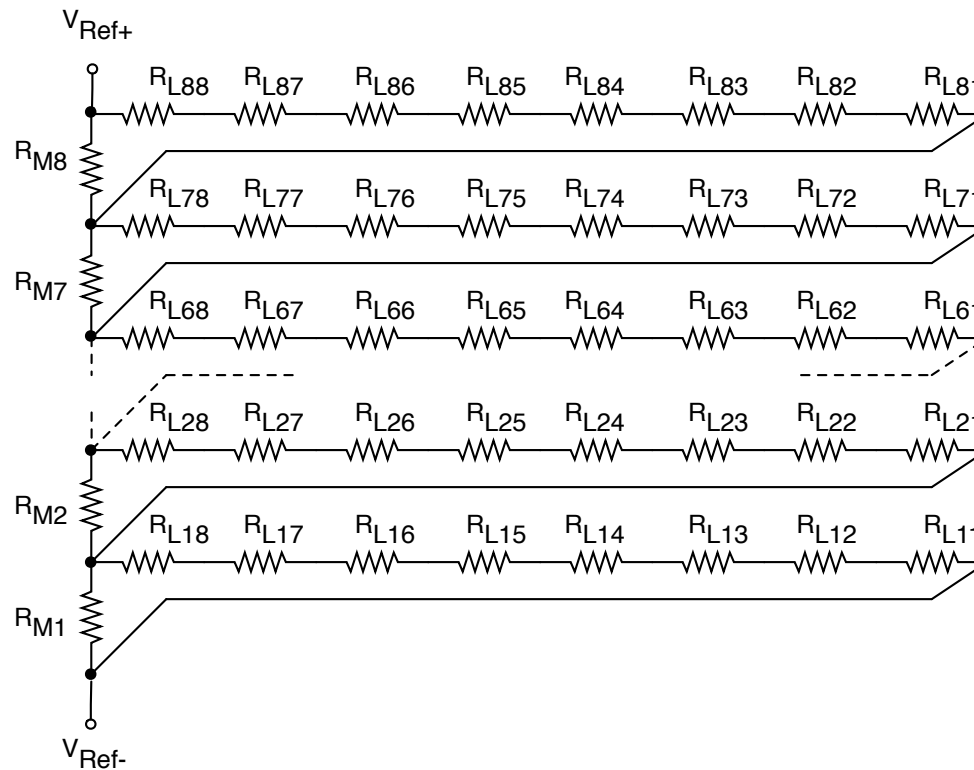
$$V_{out}(t) = V_{in}(0^-) + SR \cdot t \quad \text{for } t < t_{slew}$$

$$V_{Out}(t) = V_{in}(0^-) + \Delta V_{in}(0) - \Delta V \cdot e^{-t/\tau} \quad \text{for } t > t_{slew} \quad (6)$$

$$\Delta V = SR \cdot \tau; \quad t_{slew} = \frac{\Delta V_{in}(0)}{SR} - \tau,$$

non-linear time-response!

X-Y Selection with Shunt Resistances



$$R_{eq} = \frac{kR_U R_s}{kR_U + R_s}. \quad (7)$$

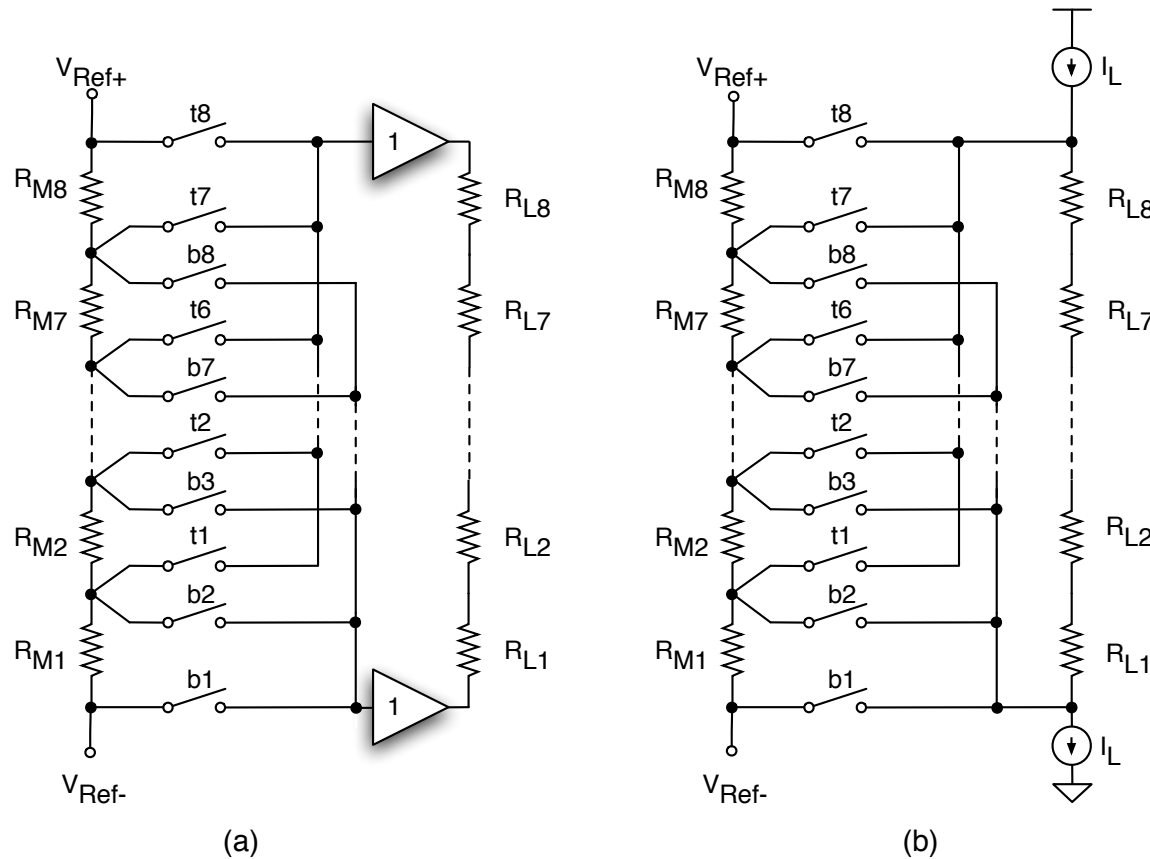
If linearity is an issue remember the ...

Observation

A code dependent settling of the output voltage causes distortion. High *SFDR* requires low resistances at every node. The variation of the settling time must be much smaller than the hold period.

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Segmented Architectures



$$I_L = \frac{\Delta V_{LSB}}{2^{n_{LSB}} R_L} = \frac{V_{Ref+} - V_{Ref-}}{2^{n_{MSB}} \cdot 2^{n_{LSB}} R_L}. \quad (8)$$

Effect of the Mismatch

$$R_i = R_u(1 + \epsilon_a) \cdot (1 + \epsilon_{r,i}), \quad (9)$$

ϵ_a is the absolute error and $\epsilon_{r,i}$ is the relative mismatch.

$$V_{out}(k) = V_{Ref} \frac{\sum_0^k R_i}{\sum_0^{2^n-1} R_i}; \quad k = 0, \dots, 2^n - 1. \quad (10)$$

$$V_{out}(k) = V_{Ref} \frac{k + \sum_0^k \epsilon_{r,i}}{2^n - 1 + \sum_0^{2^n-1} \epsilon_{r,i}}; \quad k = 0, \dots, 2^n - 1. \quad (11)$$

The error depends on the accumulation of mismatches and is zero at the two endings of the string.

Mismatch with linear gradient

A straight string with unity elements spaced by ΔX and gradient α in their relative values gives

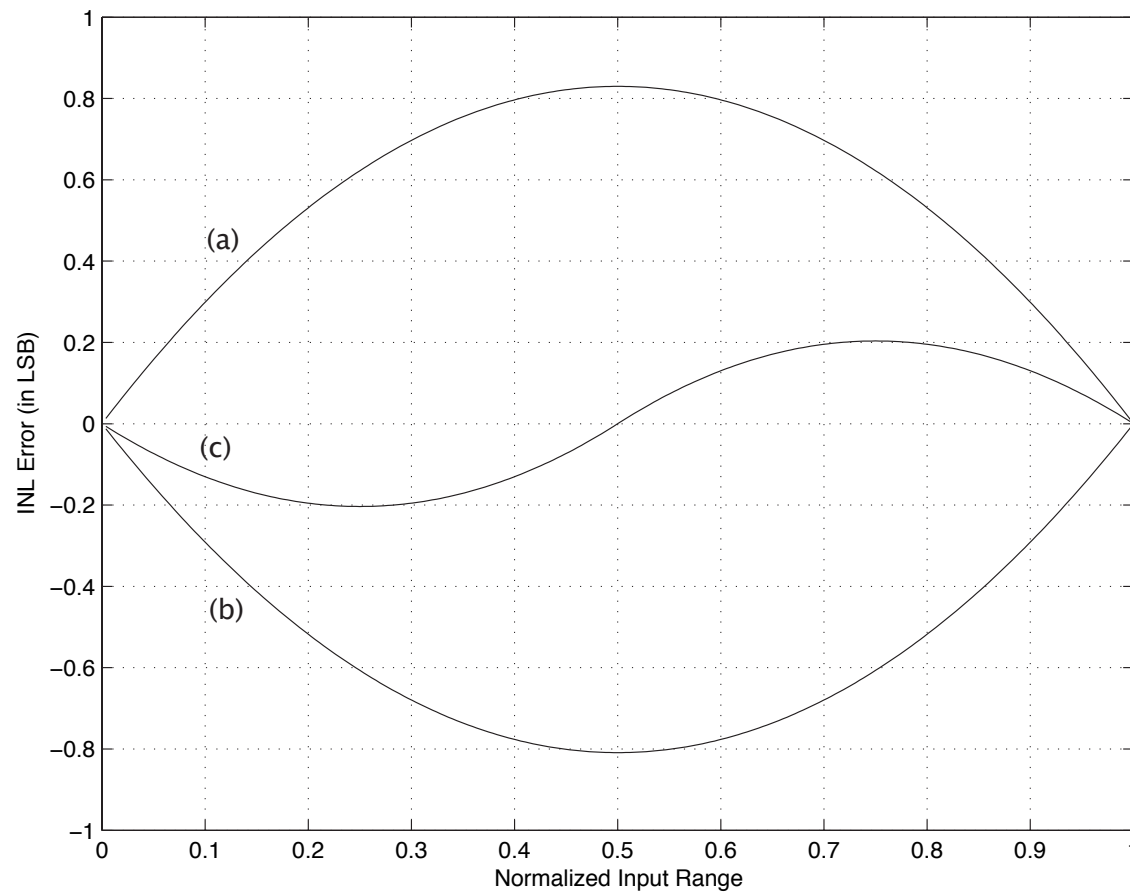
$$R_k = R_0(1 + k \cdot \alpha \Delta X); \quad k = 0, \dots, 2^n - 1 \quad (12)$$

and the output at the tap k becomes

$$V_{out}(k) = V_{Ref} \frac{k + \alpha \Delta X \cdot k(k + 1)/2}{2^n - 1 + \alpha \Delta X \cdot (2^n - 1)2^n/2} \quad (13)$$

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INL with Linear Gradient: straight and Folded Line



Example: Harmonic Distortion caused by a linear Grading

Consider a $2.5 \cdot 10^{-5} / \mu$ gradient (α) in the resistivity of a straight string of resistors spaced by 4μ .

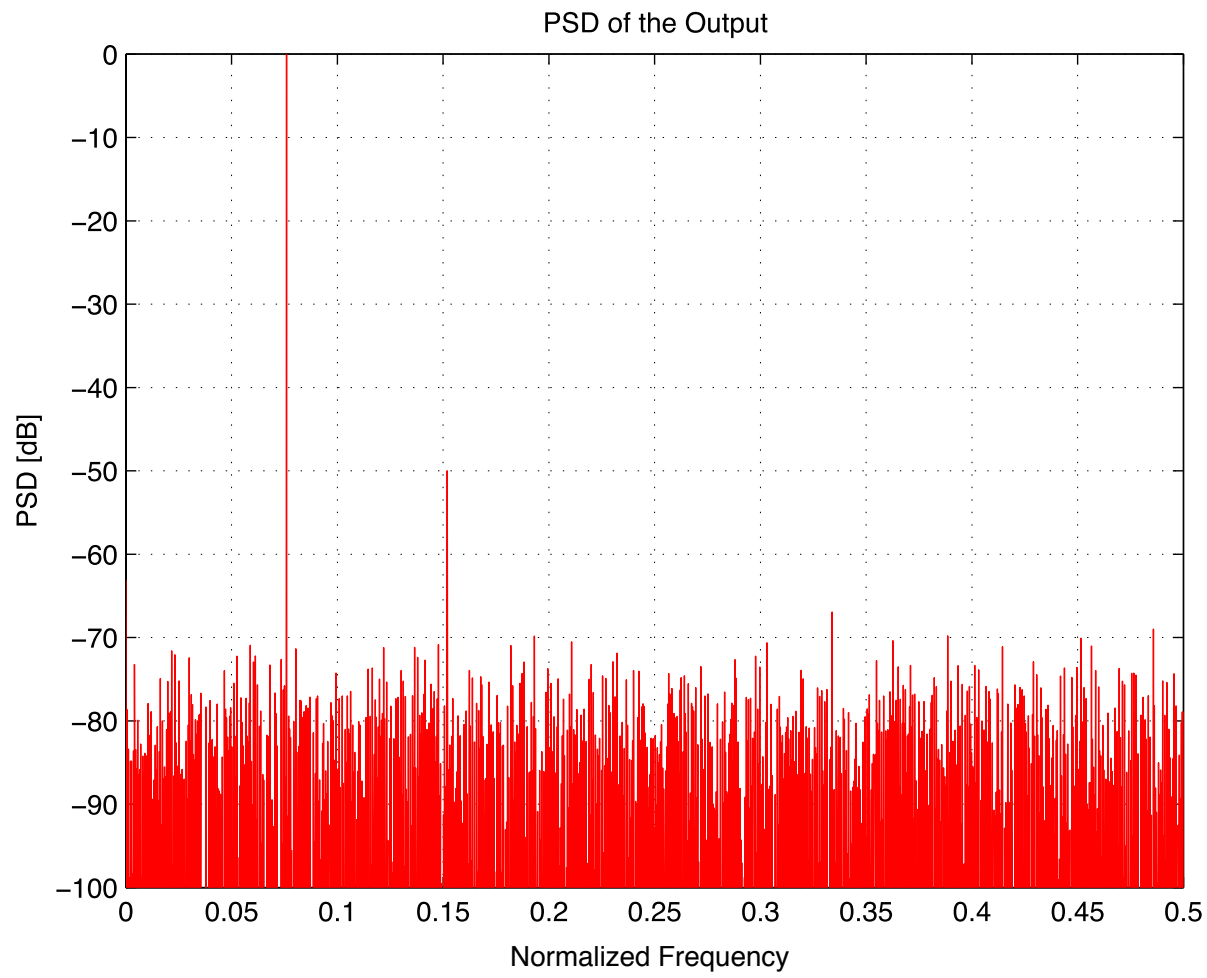
The DAC is an 8-bit Kelvin divider connected between 0 V and 1 V.

The fft of an input sequence made by 2^{12} points gives for an 8-bit DAC a noise floor at

$$P_Q = -1.78 - 6.02 \cdot 8 - 10 \cdot \log(2048) = -83 \text{ dB};$$

enough seeing for spurs higher than -65 dB (18 dB above the noise floor).

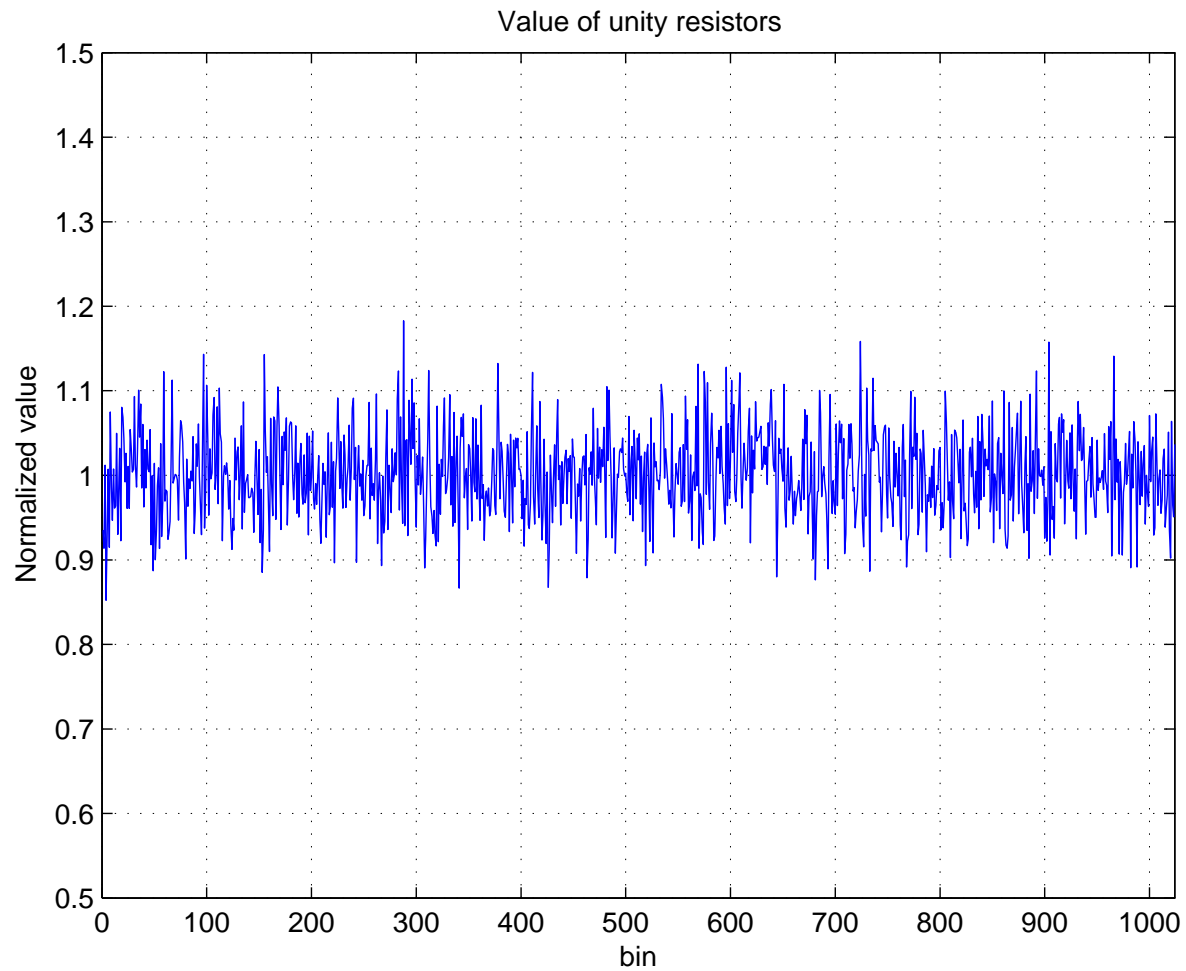
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Trimming and Calibration

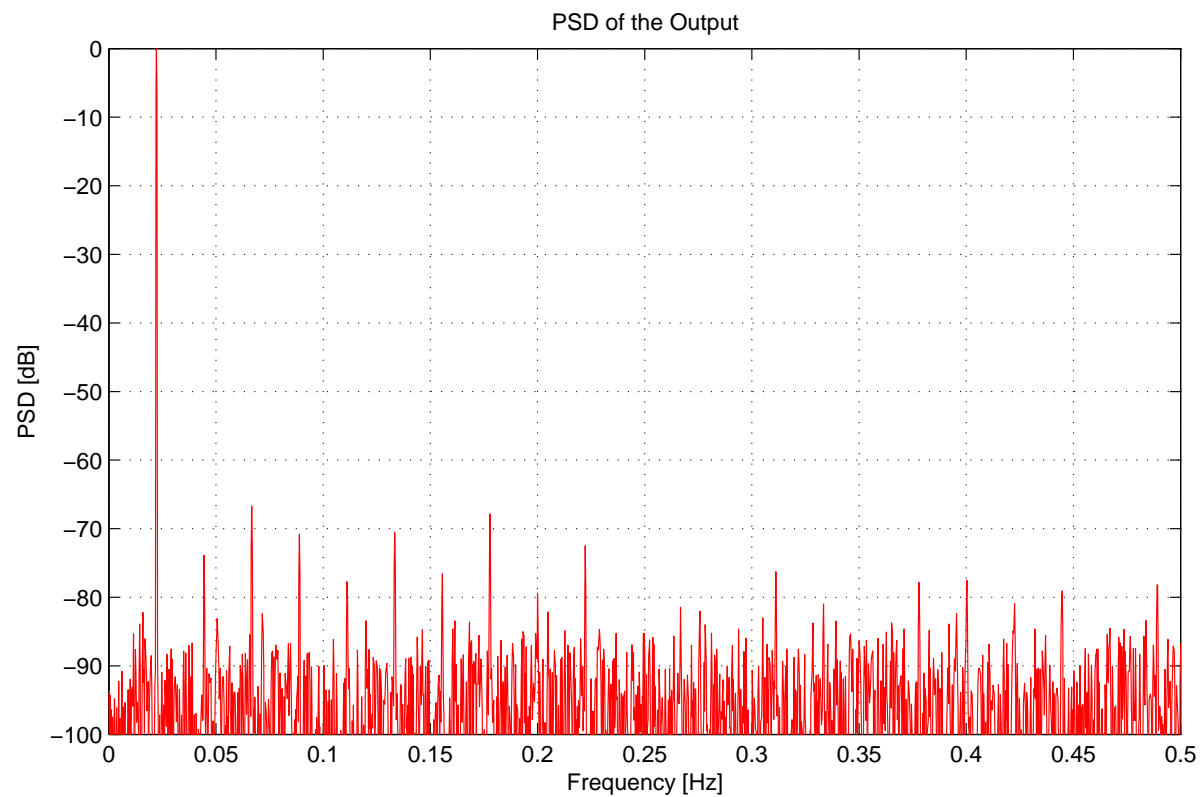
- Trimming statically corrects the mismatches due to the fabrication process inaccuracies.
- Use of thin film technology that realizes resistors on the top of the passivation layer of the integrated circuit for precisely adjust values at the wafer level using a laser.
- Use of fuses or anti-fuses for opening or closing the interconnections of a network of resistive elements.
- Correction with fuses or anti-fuses is done during testing (either before or after packaging) and is permanent.

Example: Effect of random mismatch on resistors



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Spectral distortion

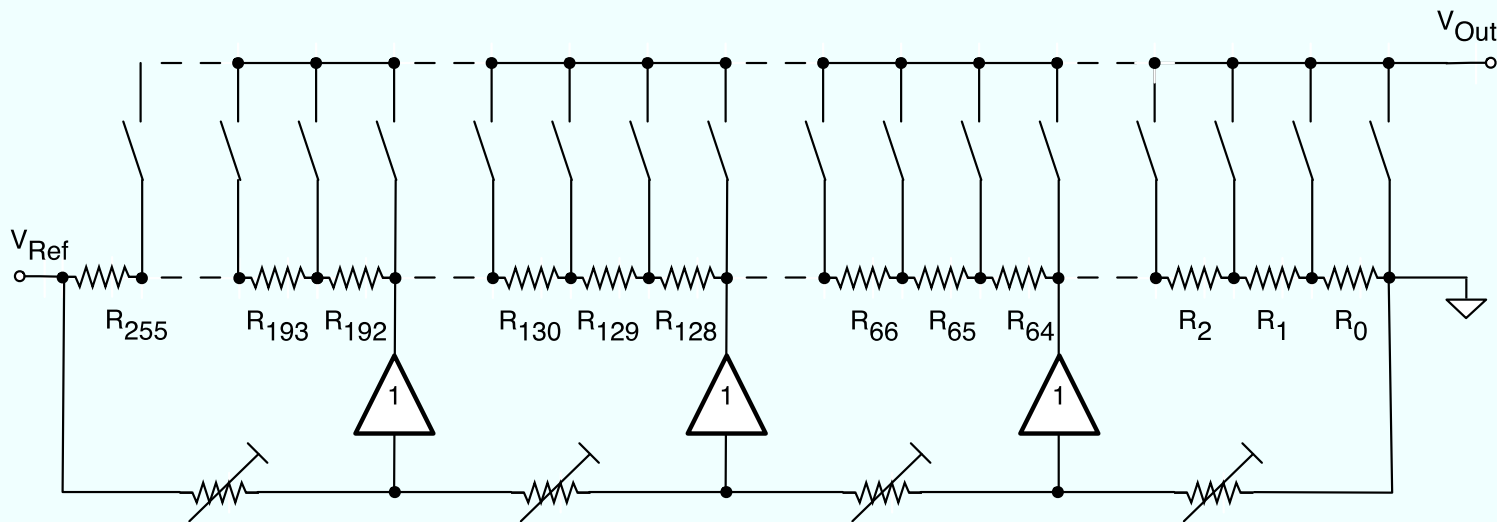


Calibration

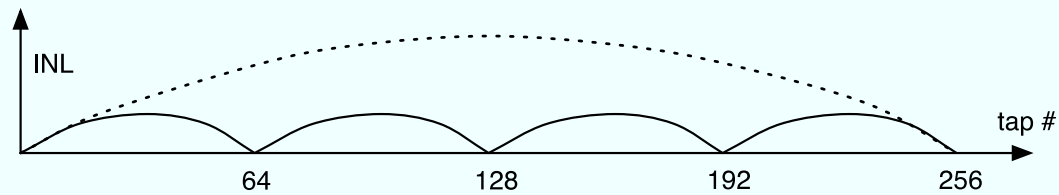
- Use of fuses or anti-fuses for achieving calibration at the wafer level or after packaging.
- Use of switches exercised by digital controlled circuits whose setting is defined at power-on (**off-line calibration**) or during the normal operation of the converter (**on-line calibration**).
- Not permanent correction that compensates for slow drifts, like aging or (for off-line) temperature effects.
- Correction at the group level instead than correcting all the elements.

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Three points Calibration



(a)



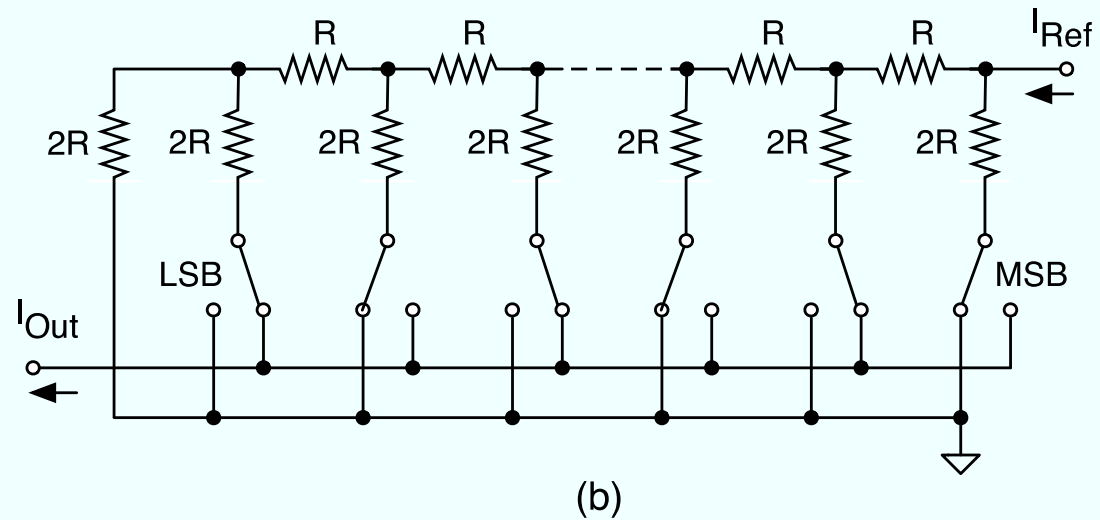
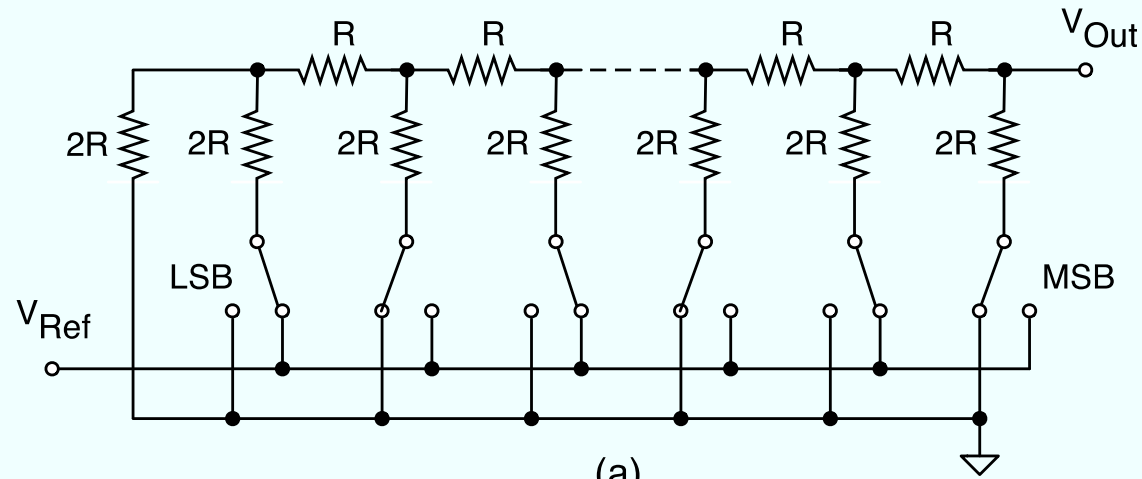
(b)

Digital Potentiometer

- Same functionality as a conventional potentiometer, except that the wiper terminal is controlled by a digital signal, so only discrete steps are allowed.
- Selection of the wiper position controlled via an n-bit register value.
- Communication and control of the device can be supported by a parallel or serial interface.
- Volatile or non-volatile logic to retain the wiper setting. For volatile logic the wiper is normally set at the mid-tap at power-up.

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R-2R Resistor Ladder DAC



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- $R-2R$ ladder reduces the total number of resistors from 2^n to $\sim 3n$.
- $R-2R$ The ladder can generate either a voltage or a current.

Voltage Mode

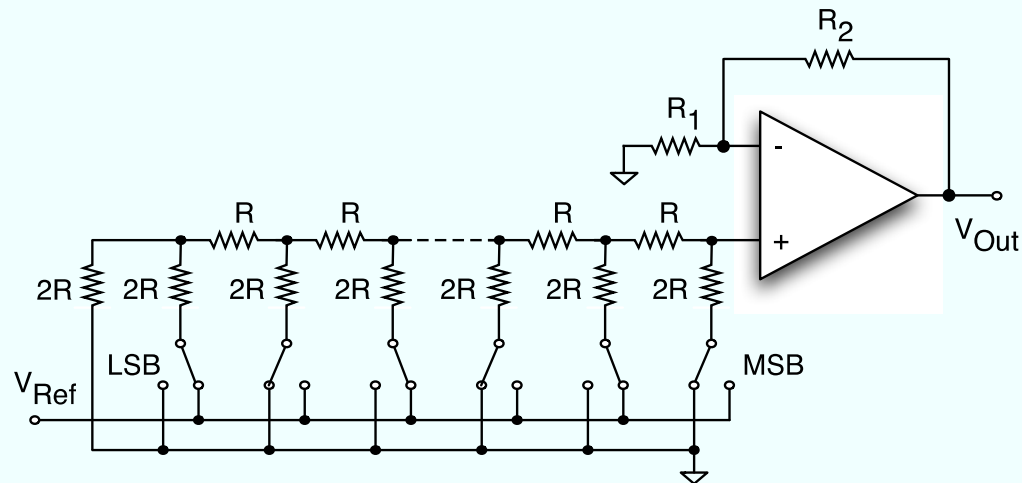
It can be verified that connecting the n -th switch to V_{Ref} leads to a contribution $V_{Out} = V_{Ref}/2^n$.

$$V_{Out} = \frac{V_{Ref}}{2}b_{n-1} + \frac{V_{Ref}}{4}b_{n-2} + \dots + \frac{V_{Ref}}{2^{n-1}}b_1 + \frac{V_{Ref}}{2^n}b_0, \quad (14)$$

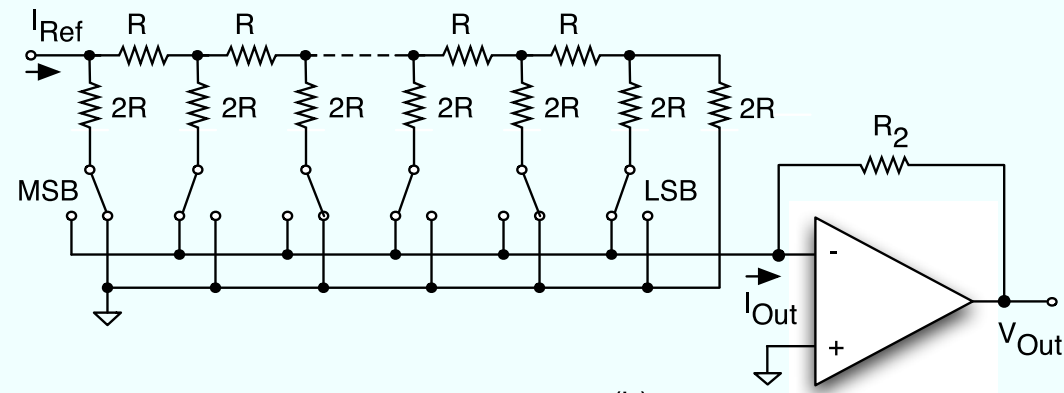
The output of the $R-2R$ ladder in the voltage mode is the superposition of terms that are the successive division of V_{Ref} by 2.

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R-2R ladder network with Op-Amp



(a)



(b)

Limits of the R-2R Network

About the reference output resistance ...

Be Aware

A code dependent load of a voltage source causes harmonic distortion. Use reference generators whose output impedance is much lower than the load in any conditions!

The input-output characteristics of the *R-2R* ladder network (either voltage or current mode) is not intrinsically monotonic.

Current Mode

The current-mode circuit performs a successive division by two of the reference current I_{Ref} provided that the voltage at the output node is ground.

The superposition of the currents selected by the switches forms the output current

$$I_{Out} = \frac{I_{Ref}}{2}b_{n-1} + \frac{I_{Ref}}{4}b_{n-2} + \dots + \frac{I_{Ref}}{2^{n-1}}b_1 + \frac{I_{Ref}}{2^n}b_0 \quad (15)$$

which is the DAC conversion of a digital signal $\{b\}$ with current output.

- 😊 $R-2R$ the parasitic capacitance of the switched node remains at the same voltage independent of the code.
- ☹ Glitches can affect the dynamic response of the current-mode implementation.

Current Mismatch

Mismatch is problematic for the current mode circuit as an error in the binary division can cause non monotonicity.

Consider the switching at the mid-scale $I_{ref}(1/2 - 1/2^n) \rightarrow I_{ref}/2$. If

$$I_{ref}(1 + \epsilon)(1/2 - 1/2^n) \rightarrow I_{ref}(1 - \epsilon)/2; \quad (16)$$

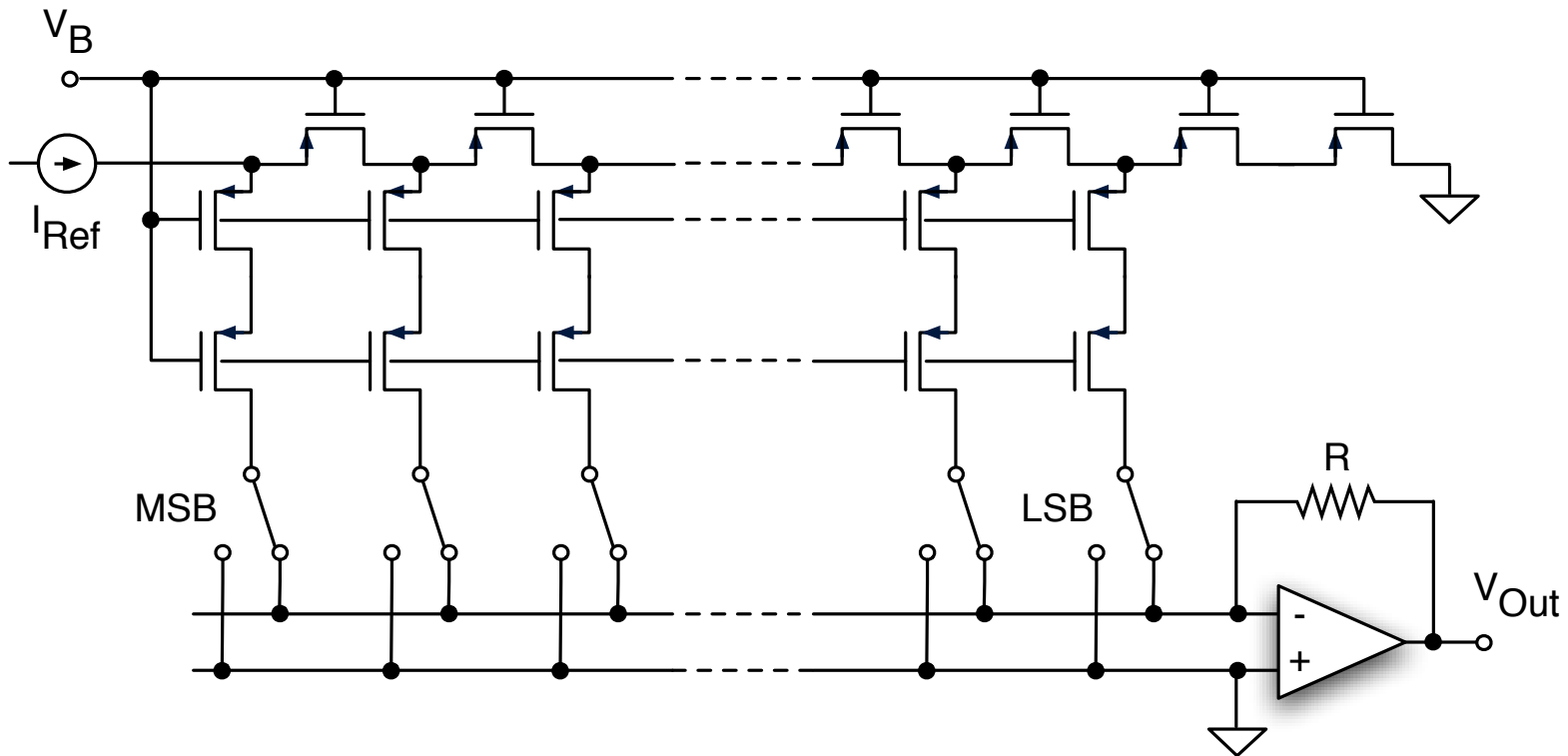
the step amplitude is

$$\Delta I \simeq I_{ref}(1/2^n - \epsilon). \quad (17)$$

if $\epsilon > 1/2^{n+1}$ the step amplitude is negative and the transfer characteristic becomes non monotonic.

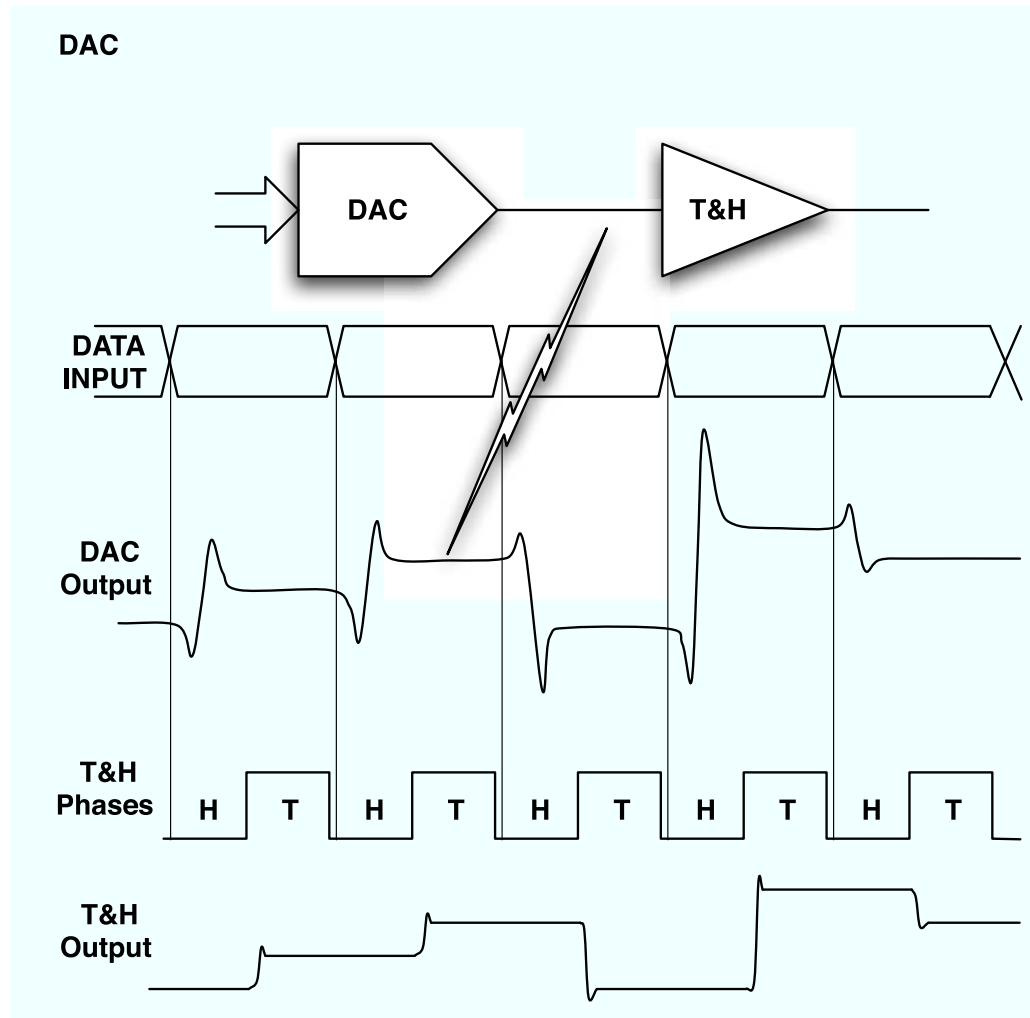
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Replacing Resistors with MOS



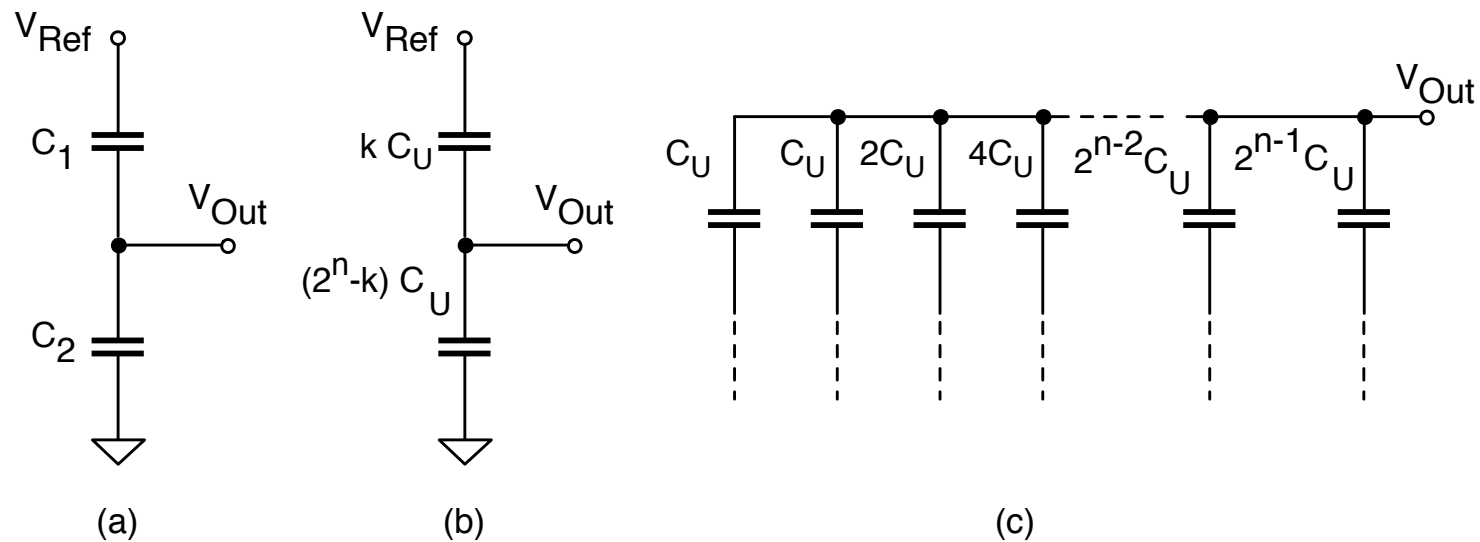
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Deglitching



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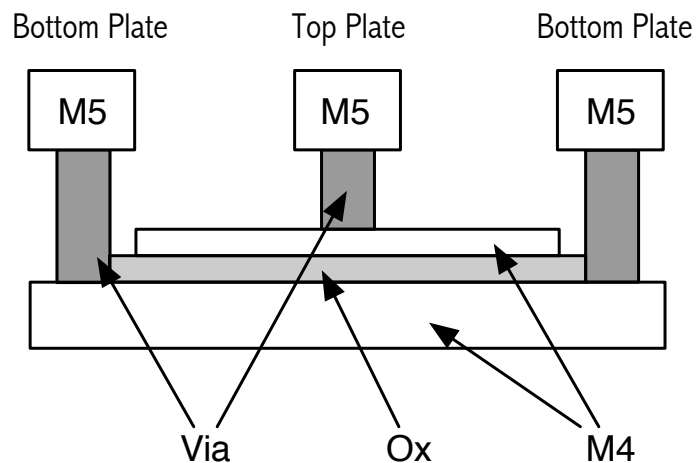
Capacitor Based Architectures



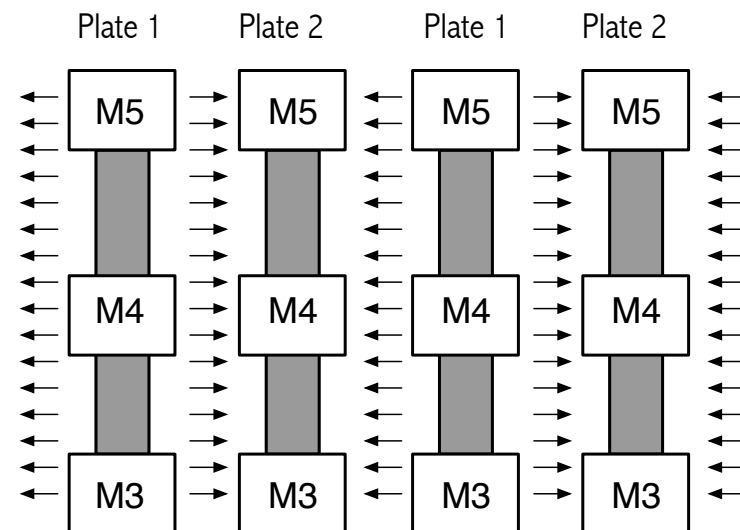
$$V_{Out} = V_{Ref} \frac{C_1}{C_1 + C_2}. \quad (18)$$

Integrated Capacitors

Integrated capacitance configurations: with plates one on the top of the other (the capacitor can be poly-oxide-poly or Metal-Insulator-Metal, *MIM* or with plates made of side by side fingers of metals and vias (Metal-Metal Comb Capacitor).



(a)



(b)

Parasitic Limitations

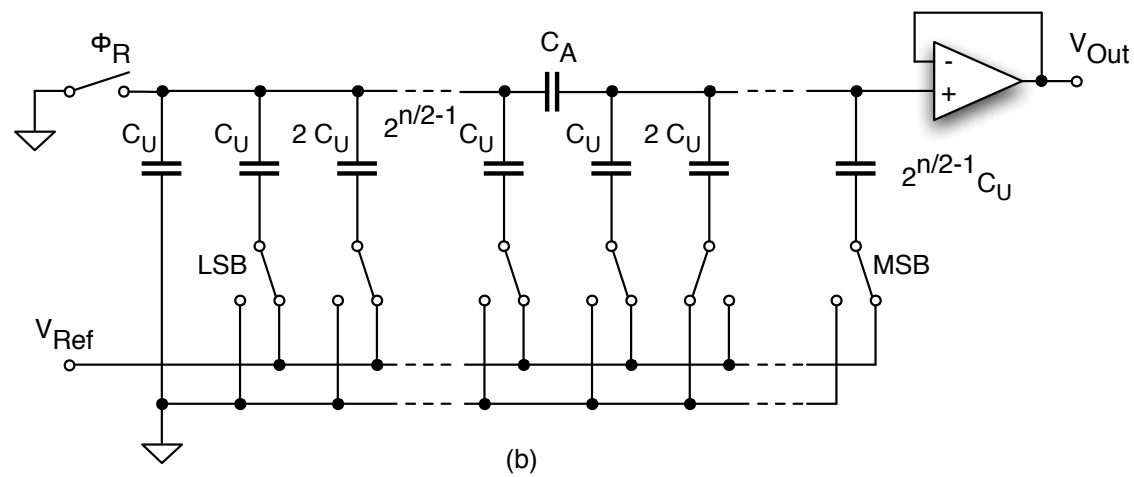
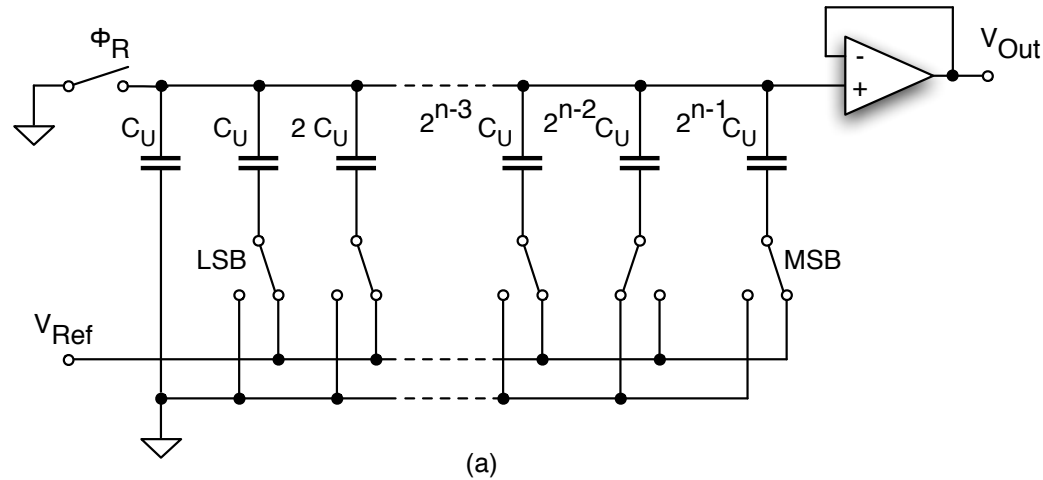
- ☺ The parasitic connected to V_{Ref} or ground receives the required charge by low impedance nodes.
- ☹ The parasitic capacitances connected to the output node changes the output voltage.

$$V_{Out} = V_{Ref} \frac{\sum_1^n b_i C_i}{\sum_0^n C_i + \sum_0^n C_{p,i}}, \quad (19)$$

- ☺ If the parasitic capacitances are independent of the output voltage equation (19) leads to a gain error only.
- ☹ Non-linear parasitics that change with the output voltage cause harmonic distortion.

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n-bit Capacitor Divider



Attenuation Capacitor

The attenuation cap C_A reduces the capacitors' count.

The biggest element of the left array is $2^{n/2-1}C_U$ instead of $\frac{1}{2}C_u$.

The condition

$$\frac{C_A \cdot 2^{n/2}C_U}{C_A + 2^{n/2}C_U} = C_u \quad (20)$$

yields the value of C_A

$$C_A = \frac{2^{n/2}}{2^{n/2} - 1}C_U. \quad (21)$$

Unfortunately the value of C_A is a fraction of C_U : obtaining the necessary accuracy requires care in the layout.

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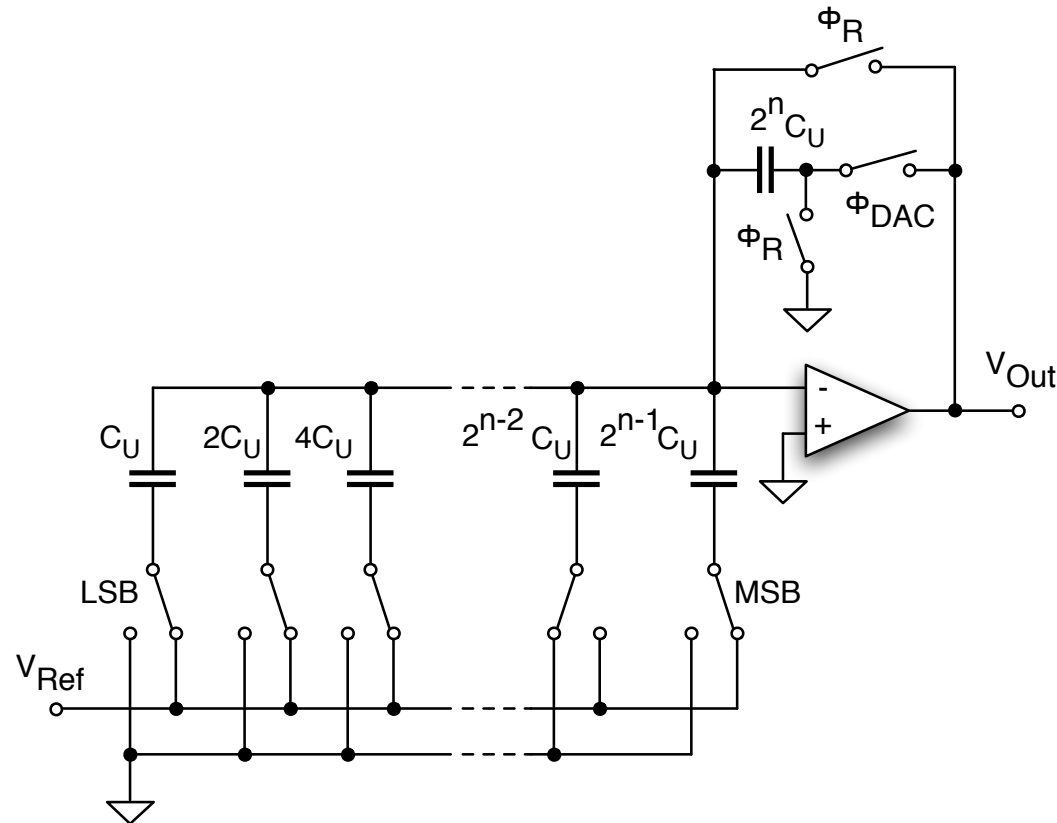
For the Op-amp used as buffer ...

Remember!

Capacitor based DAC must avoid discharging at the high impedance output node. Measure the output with a buffer or an amplifier with infinite input resistance.

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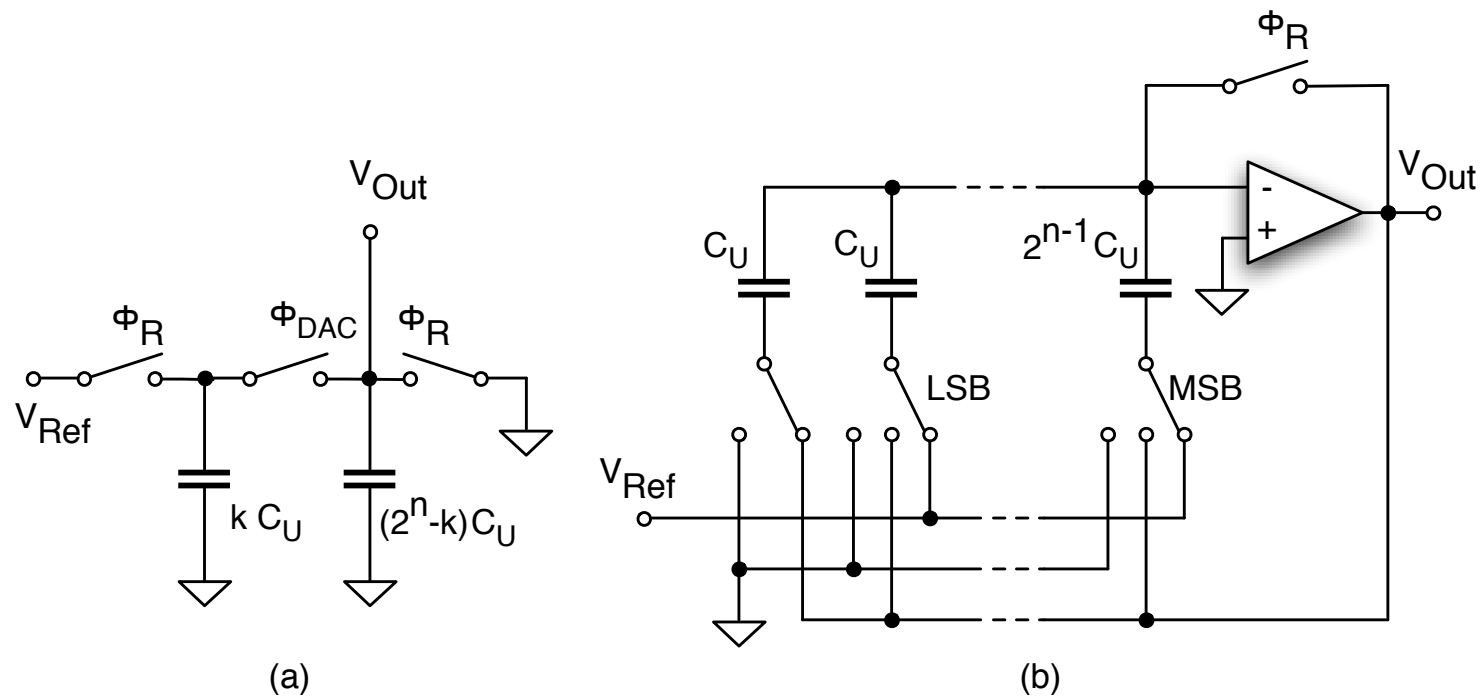
Capacitive MDAC



$$V_{Out} = -\frac{\sum_{i=0}^{n-1} b_i 2^i C_U}{2^n C_U}, \quad (22)$$

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"Flip Around" MDAC



$$V_{Out} = V_{Ref} \frac{kC_U}{2^n C_U}. \quad (23)$$

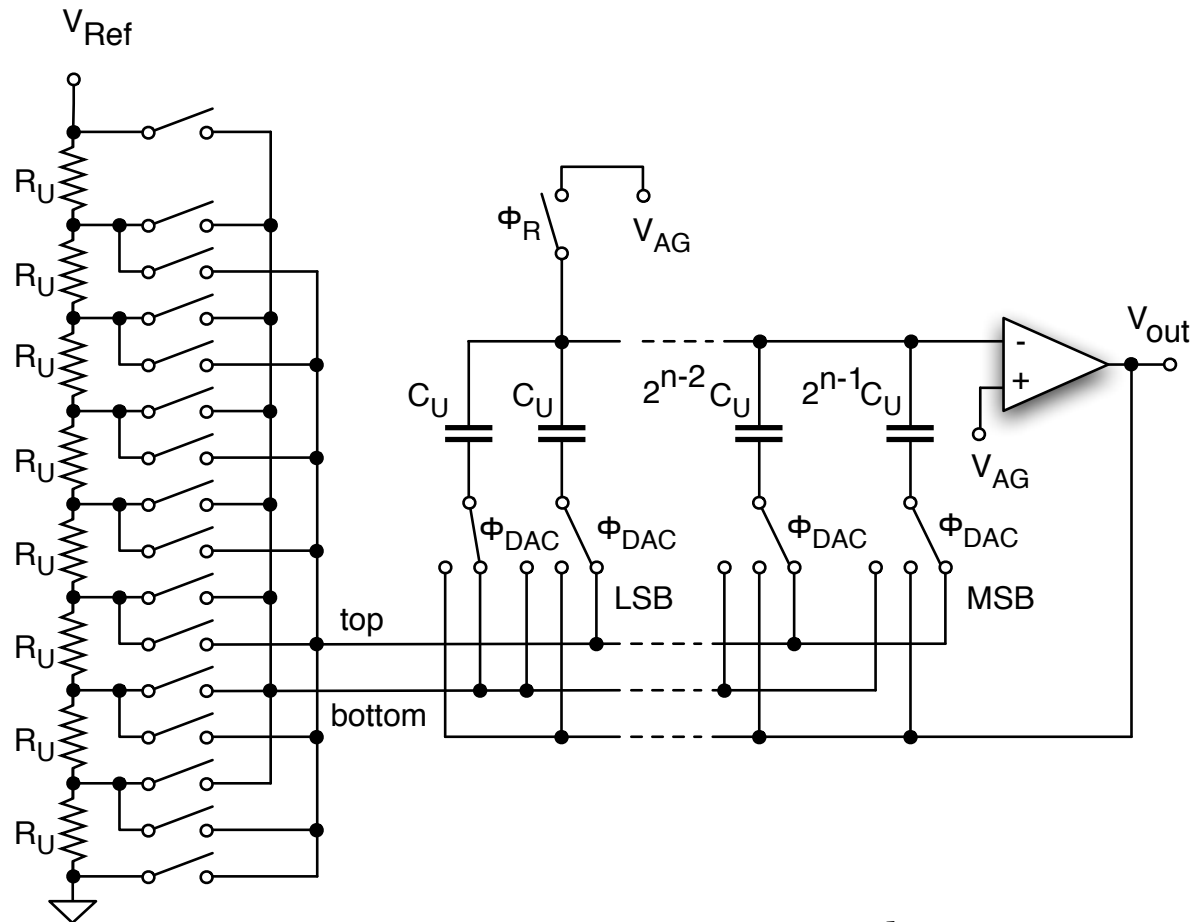
When using capacitors always

Keep in Mind

Any capacitor-based architecture requires a reset phase to make sure that the array is initially discharged. Since the output voltage is not valid during the reset, a track and hold sustains the output.

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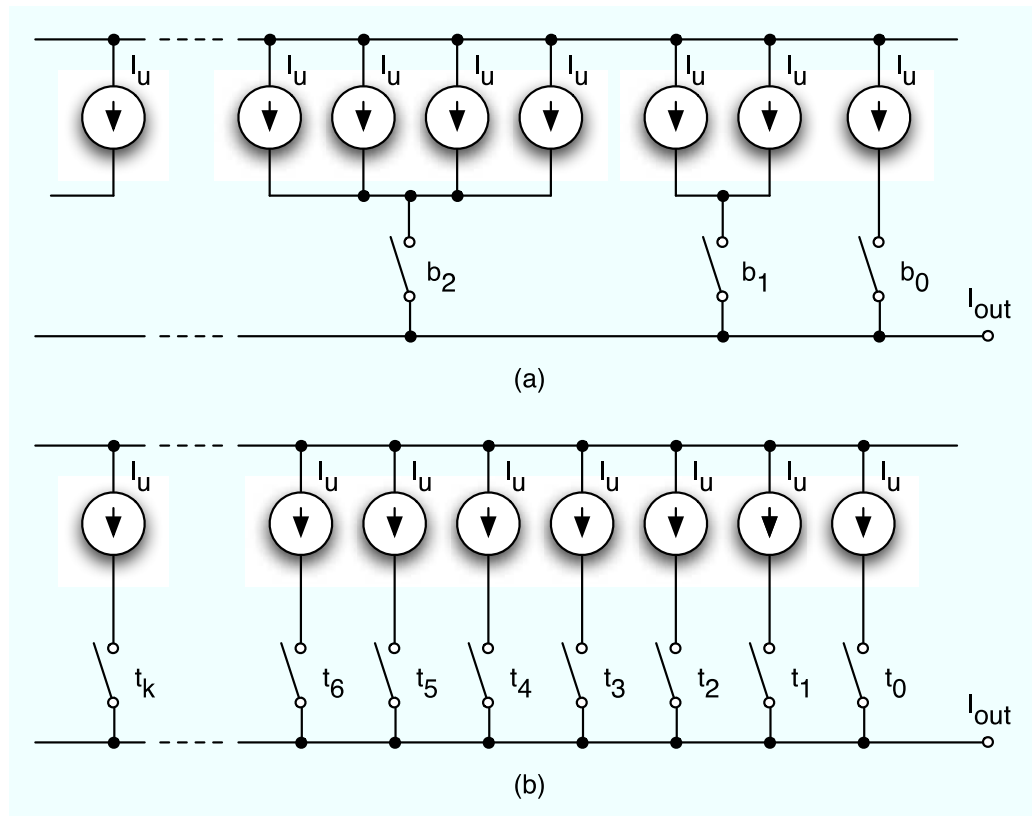
Hybrid Capacitive-Resistive DACs



$$V_{out} = V_{MSB} + \Delta_{MSB} \frac{k}{2^n} \quad (24)$$

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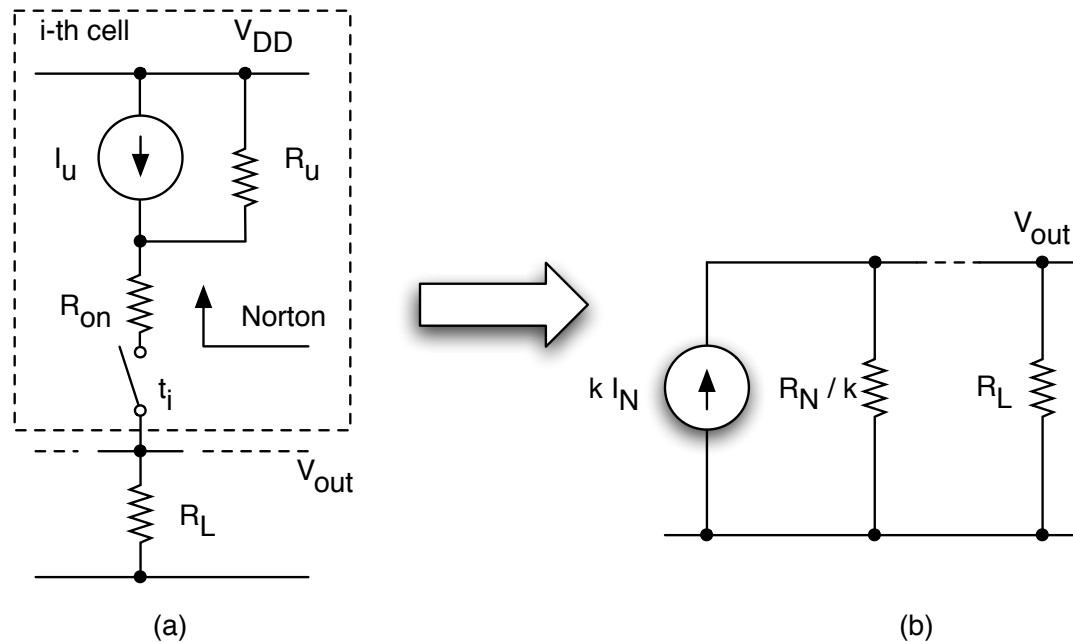
Current Source based Architectures



$$I_{out} = I_u \left[b_0 + 2b_1 + 2^2b_2 + \dots + 2^k b_k + \dots + 2^{n-1} b_{n-1} \right]. \quad (25)$$

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Simplified Model



$$I_N = \frac{I_u R_u + V_{DD}}{R_u + R_{on}}; \quad R_N = R_u + R_{on}. \quad (26)$$

$$V_{out} = k I_N \frac{R_L \cdot R_N/k}{R_L + R_N/k} = I_N R_L \frac{k}{1 + \alpha k} \quad (27)$$

$$INL(k) = \frac{k [1 + \alpha(2^n - 1)]}{1 + \alpha k} - k; \quad k = 0, \dots, 2^n - 1. \quad (28)$$

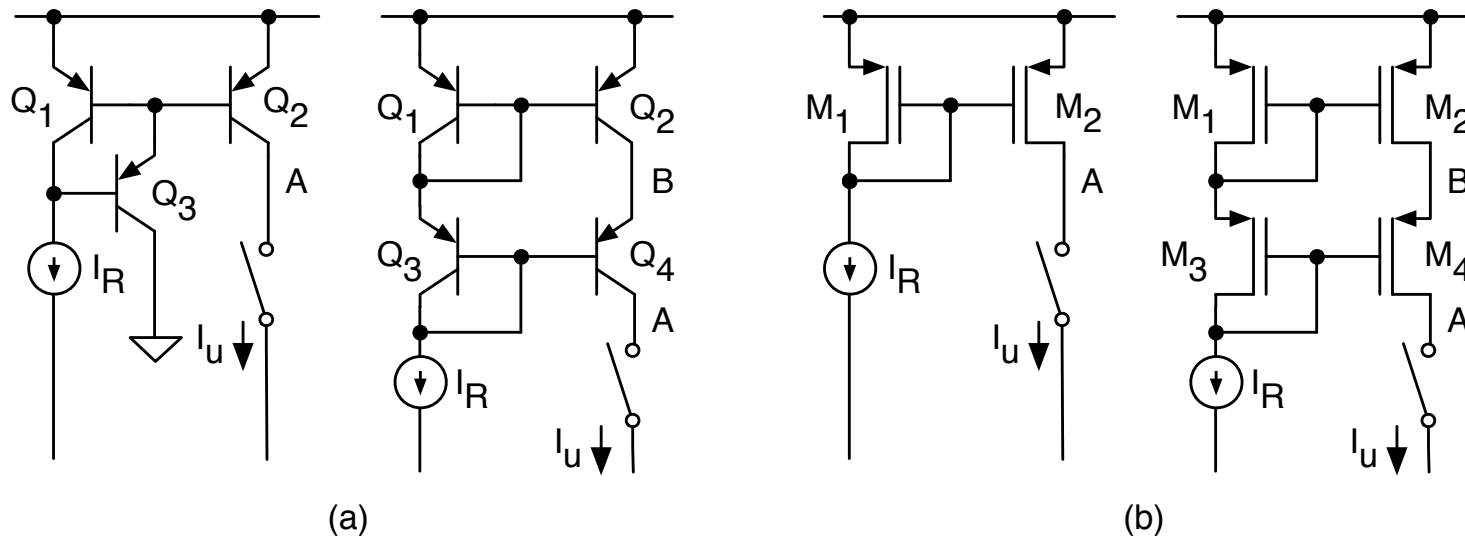
For single-ended or differential choices ...

Be Aware

The output resistance of the unity current source causes second order harmonic distortion. The use of differential architecture relaxes the requirements on the unity current source.

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Unity Current Generator



☺ Using current sources with high output resistance secures linearity.

☹ Complex schemes reduce the speed of operation.

Random Mismatch in Current Mirrors

$$I_D = \beta (V_{gs} - V_{th})^2 \quad (29)$$

$$I_1 = \bar{I} \left(1 + \frac{\Delta\beta}{\beta} + \frac{2\Delta V_{th}}{V_{gs} - V_{th}} \right) \quad (30)$$

$$I_2 = \bar{I} \left(1 - \frac{\Delta\beta}{\beta} - \frac{2\Delta V_{th}}{V_{gs} - V_{th}} \right) \quad (31)$$

$$\frac{\Delta I^2}{I^2} = \frac{\Delta\beta^2}{\beta^2} + \frac{4\Delta V_{th}^2}{(V_{gs} - V_{th})^2} \quad (32)$$

$$\frac{\Delta\beta^2}{\beta^2} = \frac{A_\beta^2}{WL}; \quad \Delta V_{th}^2 = \frac{A_{VT}^2}{WL} \quad (33)$$

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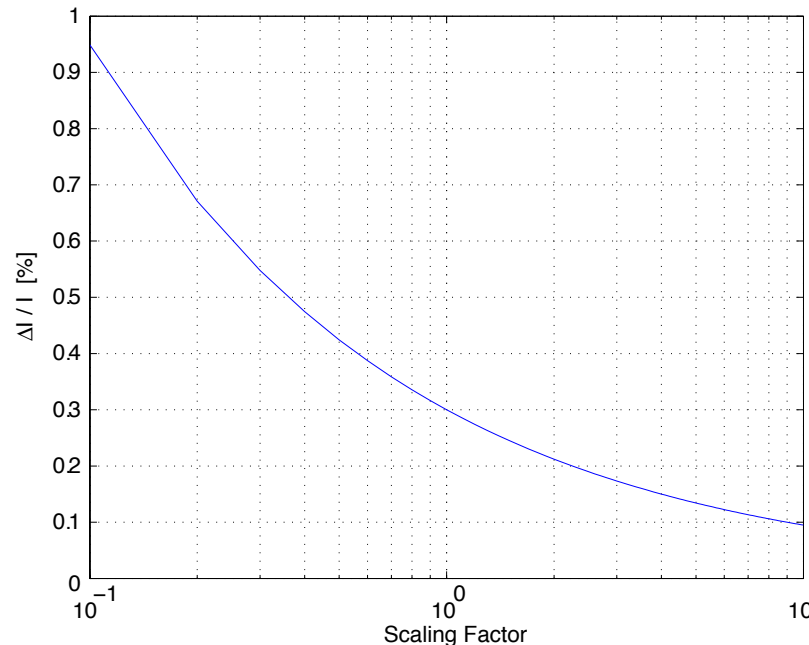
Example: Scaling of transistor sizes

The required $\Delta I/I$ for a 12-bit current steering DAC is 0.3%. μC_{ox} is $39 \mu A/V^2$, unity element is $4.88 \mu A$.

Accuracy parameters: $A_{VT} = 2 mV \cdot \mu$, $A_{\beta} = 0.3\% \cdot \mu$.

$$(WL)_{min} = \left(A_{\beta}^2 + \frac{4 \cdot A_{VT}^2}{(V_{gs} - V_{th})^2} \right) / \frac{\Delta I^2}{I^2} \quad (34)$$

$$WL = 12.11 \mu^2, \beta = I_U/V_{ov}^2 = 30.5 \mu A/V^2, W/L = 0.8.$$



Random Mismatch with Unary Selection

The endpoint-fit error for k unity current sources selected is

$$\Delta I_{out}(k) = \sum_1^k \Delta I_{r,j} - k \overline{\Delta I_r} + \sum_1^k \Delta I_{s,j} - k \overline{\Delta I_s} \quad (35)$$

Consider only the first two terms whose variance is given by

$$\Delta I_{out,r}^2(k) = k \cdot \Delta I_r^2 - \frac{k^2}{2^n - 1} \Delta I_r^2 \quad (36)$$

$$\Delta I_{out,r,max}^2 \simeq 2^{n-2} \Delta I_r^2. \quad (37)$$

If it is required that the maximum *INL* error must be lower than half *LSB* then

$$\frac{\Delta I_r}{I_u} < 2^{-n/2} \quad (38)$$

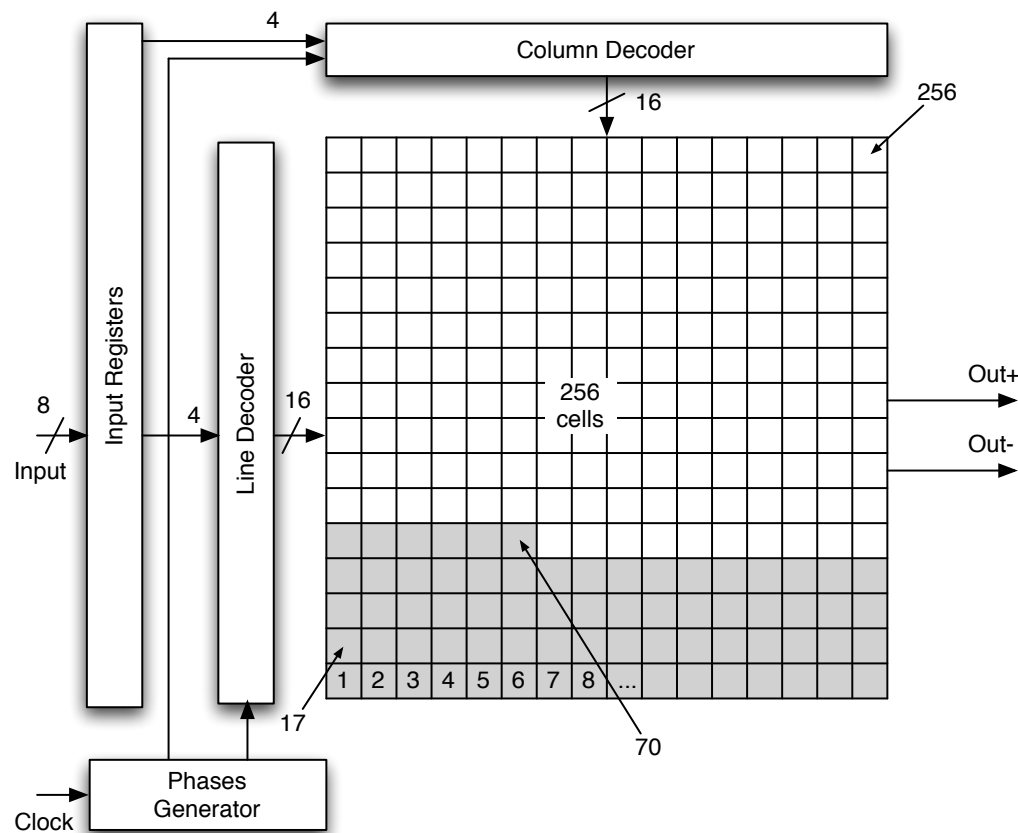
With a normal distribution of $x = \Delta I_r / I_u$ the probability of having an error equal to x is given by

$$p(x) = \frac{1}{\sigma \sqrt{2\pi}} e^{-\frac{x^2}{2\sigma^2}} \quad (39)$$

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Current Sources Selection

Unity current sources are arranged in a two-dimensional array. Sequential unary thermometric selection by lines and columns ($n \times m$) starting from one corner of the array.



Gradient Error

$$I_u(i, j) = \bar{I}_u(1 + i \cdot \gamma_x \Delta_x)(1 + j \cdot \gamma_y \Delta_y) \quad (40)$$

Maximum error is about $n/2 \cdot \gamma_x \Delta_x$ and $m/2 \cdot \gamma_y \Delta_y$ and periodic.

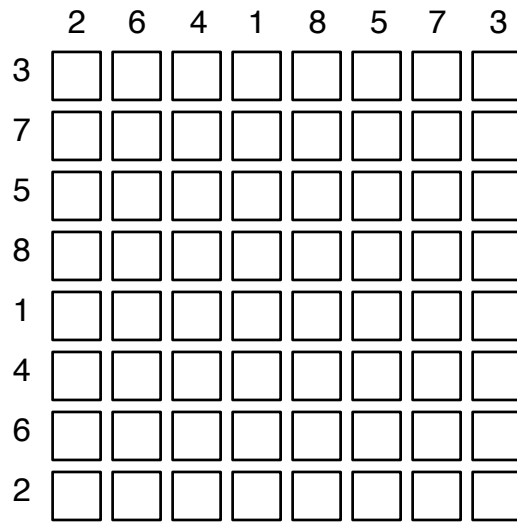
Causing INL; moreover it is worth to ...

Notice

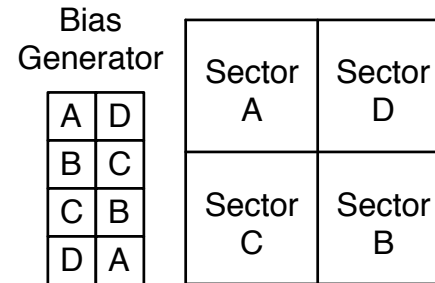
The unary selection ensures monotonicity and enables flexibility but requires one control signal per element. This makes the unary selection unpractical for 8-bit or more.

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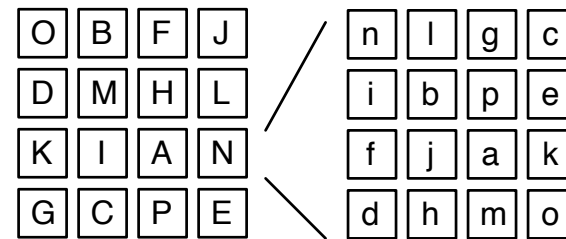
Current Sources Selection



(a)



(b)



(c)

(a) Line and column shuffling. (b) Use of multiple current references for minimizing the threshold mismatch. (c) Random walk selection of unity cells

Current Switching Methods

Binary-weighted *DAC* (combining 2^{k-1} unity current sources in parallel uses a single control for the entire parallel connection).

😊 Virtually no decoding logic is required.

😞 Possible non-monotonicity.

with a random error the maximum *DNL* (at the mid-point) is

$$DNL_{max} = \pm 2\sqrt{2^{n-1}} \Delta I_r / I_u. \quad (41)$$

DAC with unary (thermometric, shuffled, random) control.

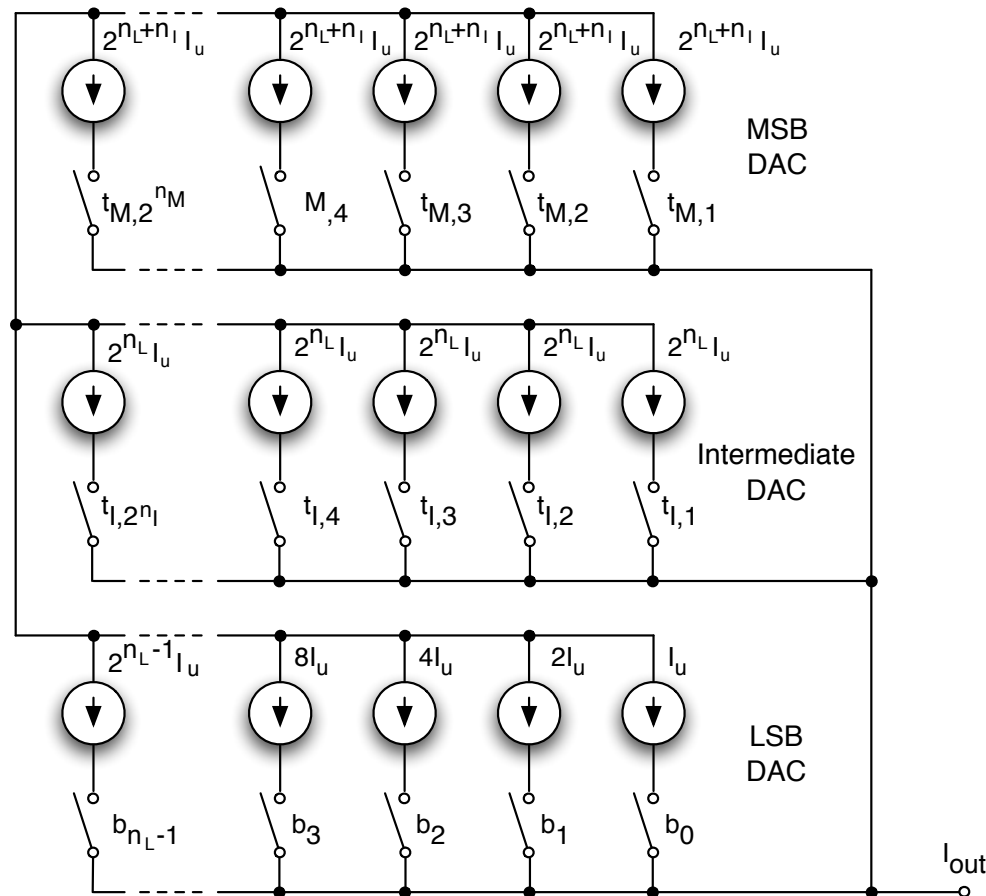
😊 Intrinsic monotonicity, minimum glitches distortion, good *DNL* and *INL*.

😞 Each unity current source requires a logic control signal.

The maximum *DNL* is $2\Delta I_r / I_u$ for any code transition.

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Segmentation



Area of Segmented DAC

The area of a segmented architecture depends on the area of the unity current sources and the area of the circuitry necessary to generate and distribute the control signals.

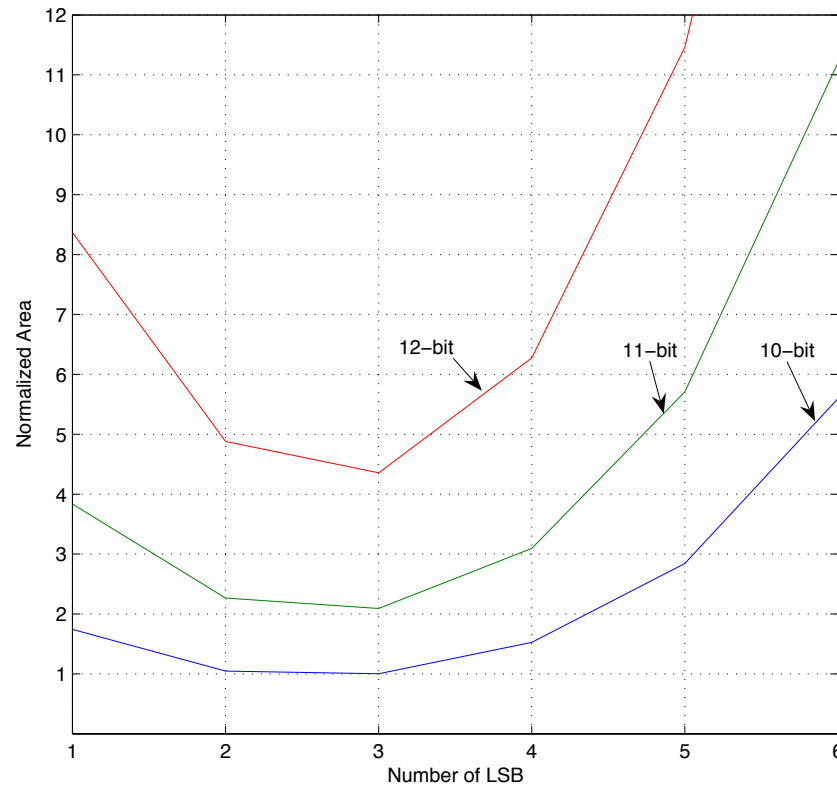
The maximum allowed *DNL* determines the value of the gate area *WL* of the *MOS* transistor used to generate I_U in the binary weighted *LSB DAC*.

$$WL > 2^{n_L+1} \left(A_\beta^2 + \frac{4 \cdot A_{VT}^2}{(V_{gs} - V_{th})^2} \right) / DNL_{max}^2 \quad (42)$$

$$A_{DAC} = 2^n \cdot A_u \cdot 2^{n_L} + A_d \cdot n_M 2^{n_M} \quad (43)$$

$$A_{DAC} = 2^n \cdot A_u \left(2^{n_L} + \frac{A_d n - n_L}{A_u 2^{n_L}} \right). \quad (44)$$

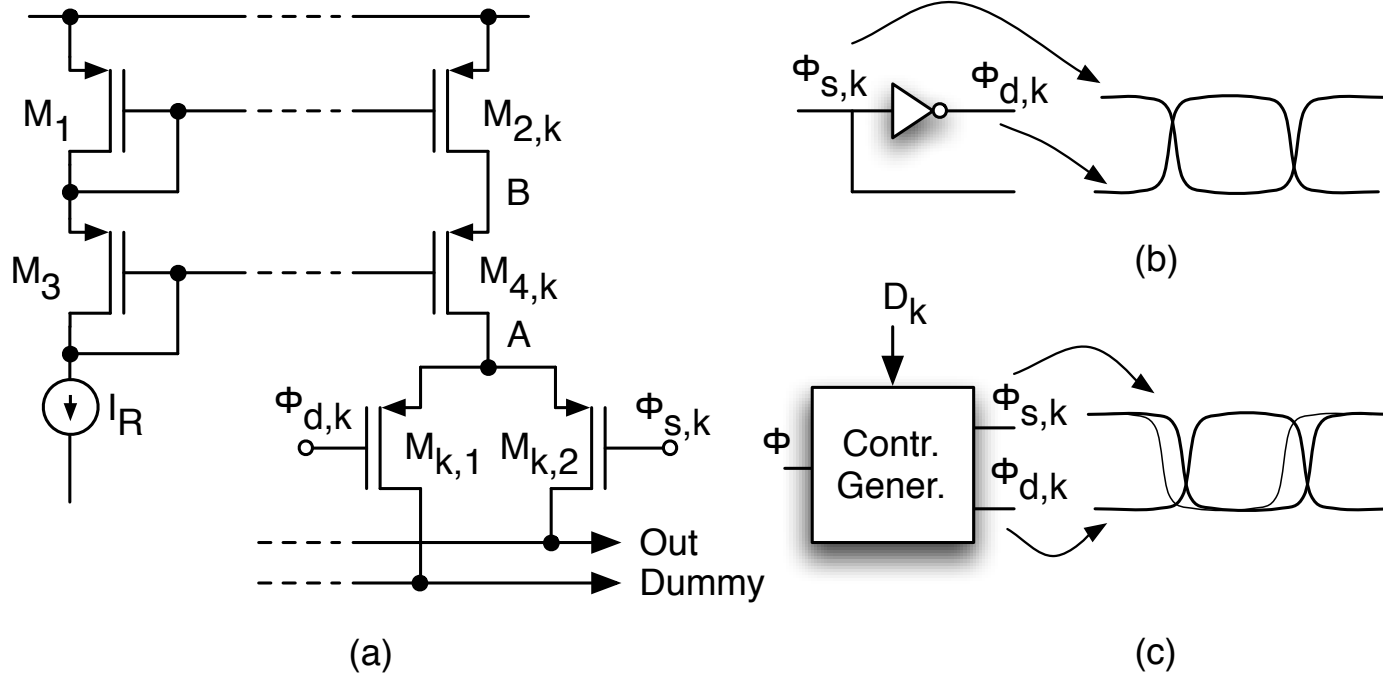
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A double segmentation further reduces the logic area.

$$A_{DAC} = 2^n \cdot A_u \left[2^{n_L} + \frac{A_d}{A_u 2^n} (n_I 2^{n_I} + n_M 2^{n_M}) \right]. \quad (45)$$

Switching of Current Sources



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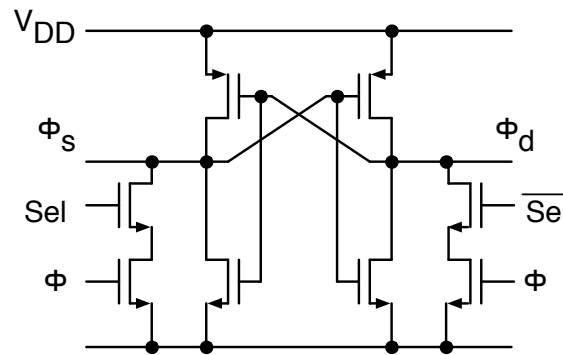
When generating the control phases ...

Remember!

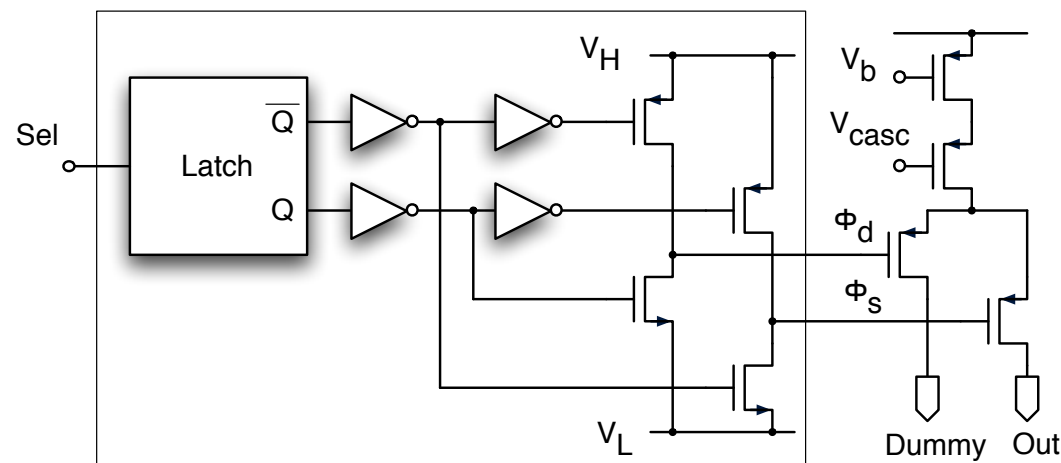
Never (not even for a short-time), leave the connection of a unity current generator open. The transistors making it would go into the triode region with a long recovery time.

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Switching Phase Generator



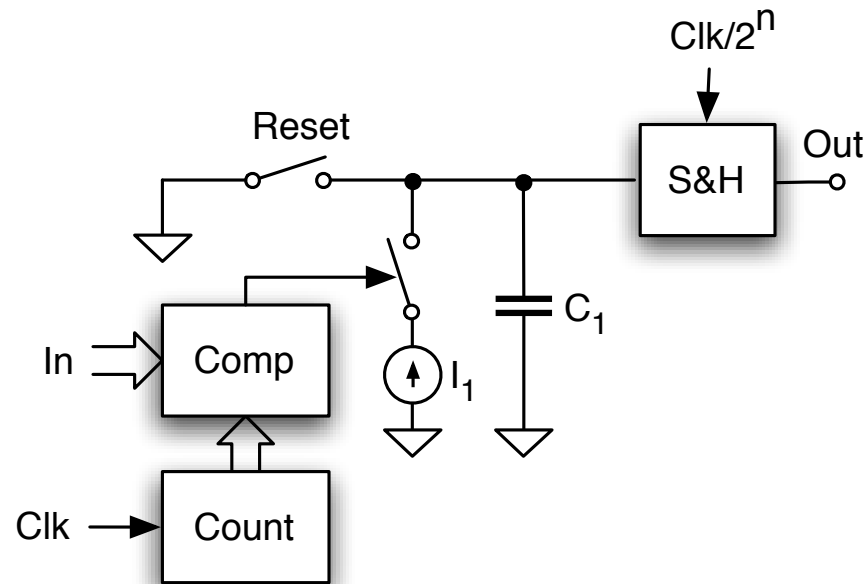
(a)



(b)

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Other Architectures

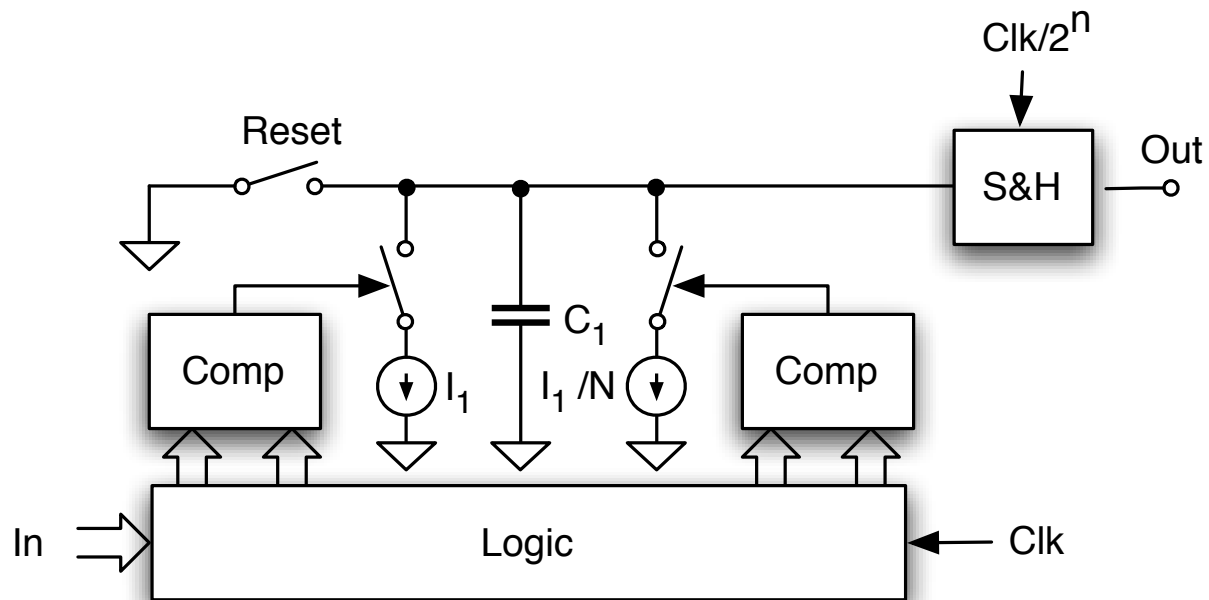


Single ramp DAC

$$V_{out} = \frac{kI_1}{C_1 f_s}. \quad (46)$$

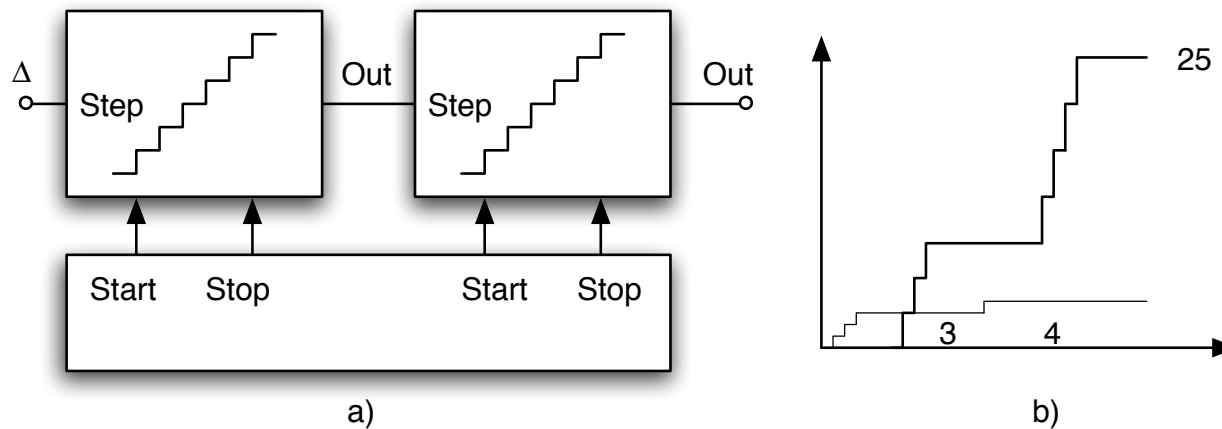
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Other Architectures (ii)



Dual-ramp DAC

Other Architectures (iii)

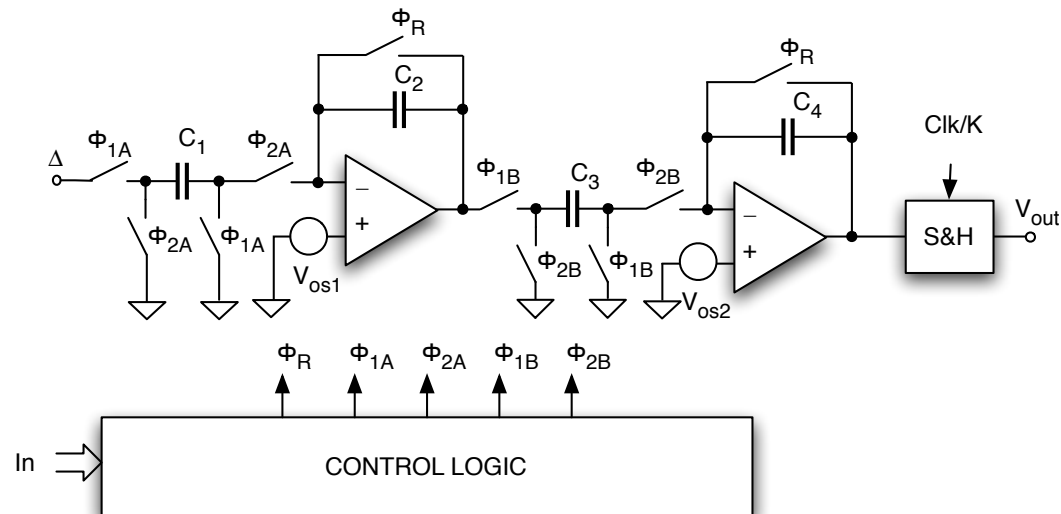


Algorithmic converter and its possible output waveform

$$k = p_1 \cdot x + p_2 \cdot y; \quad p_1 < p_2 \quad (47)$$

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Other Architectures (iv)



Possible circuit implementation of the algorithmic converter

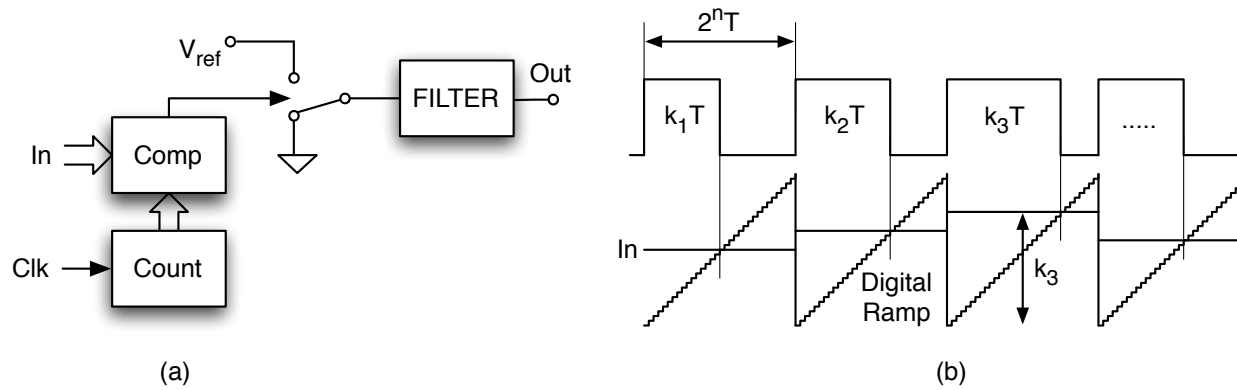
$$V_{out1} = p_1(\Delta - V_{os1}) + V_{os1} \quad (48)$$

$$\Delta V_{out2} = p_1(\Delta - V_{os1}) + V_{os1} - V_{os2} \quad (49)$$

$$x + y = const \quad (50)$$

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Other Architectures (v)



(a) Duty-cycle DAC. (b) signal waveforms.

Wrap-up

We studied digital-to-analog architectures used in integrated circuits.

The first step is considering the basic requirements on the voltage and the current references as the accuracy of any DAC (and also any ADC) critically depends on the quality of its references.

We should know features and limits of resistor based and capacitor based architectures that provide an attenuation of the reference voltage under the control of the digital input.

We should also know about DAC architectures based on the steering of unary or binary-weighted current sources.

Finally some other architectures out of many possible have been discussed.