Circuit Realization for Data Weighted Averaging (DWA)

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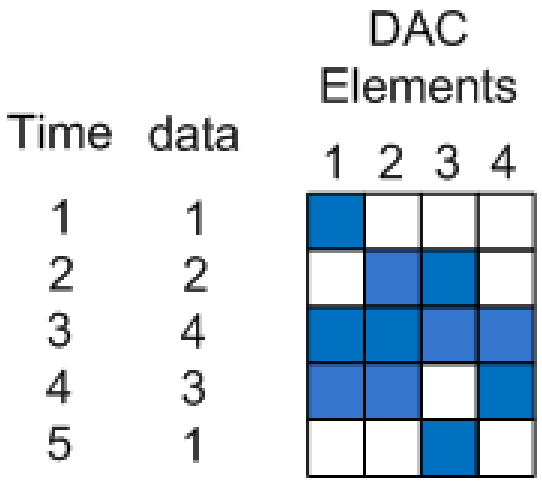
A ΔΣ modulator with multi-bit quantizer

- To improve the stability of the modulator
- To improve the SQNR under low OSR
- DEM to linearize the DAC at the modulator input
- Data weighted averaging (DWA) is a very effective and simple way to linearize the feedback DAC

The DWA algorithm

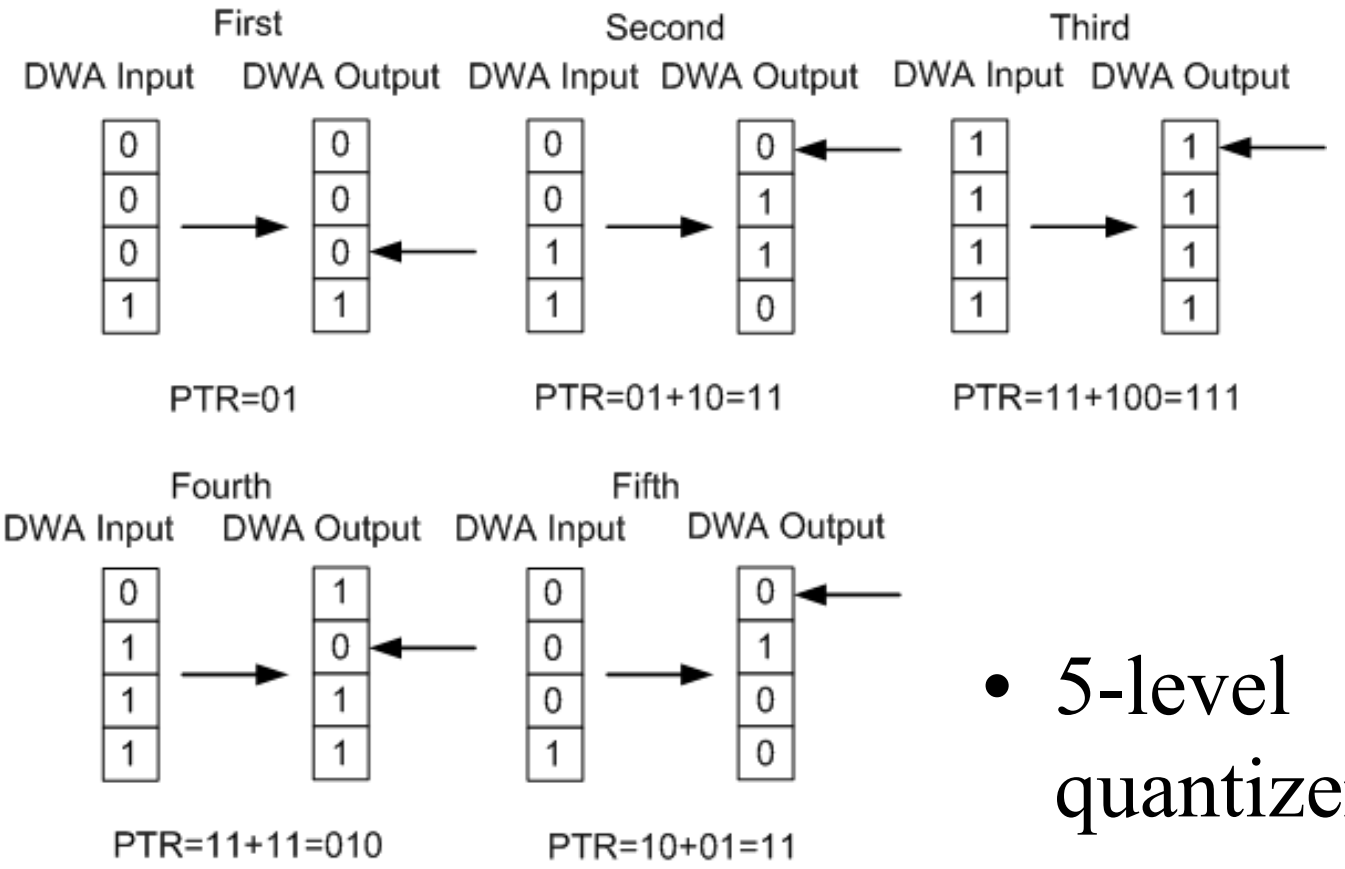


- Rotation of the thermometer code
- First order noise shaping for DAC mismatch

DWA implementation

- A DWA system contains two important building blocks
- The first one is the pointer which indicates which unit element shall be used as the starting point in a DAC operation
- The second one is a shifter which maps the relationship between the thermometer code and DAC unit elements

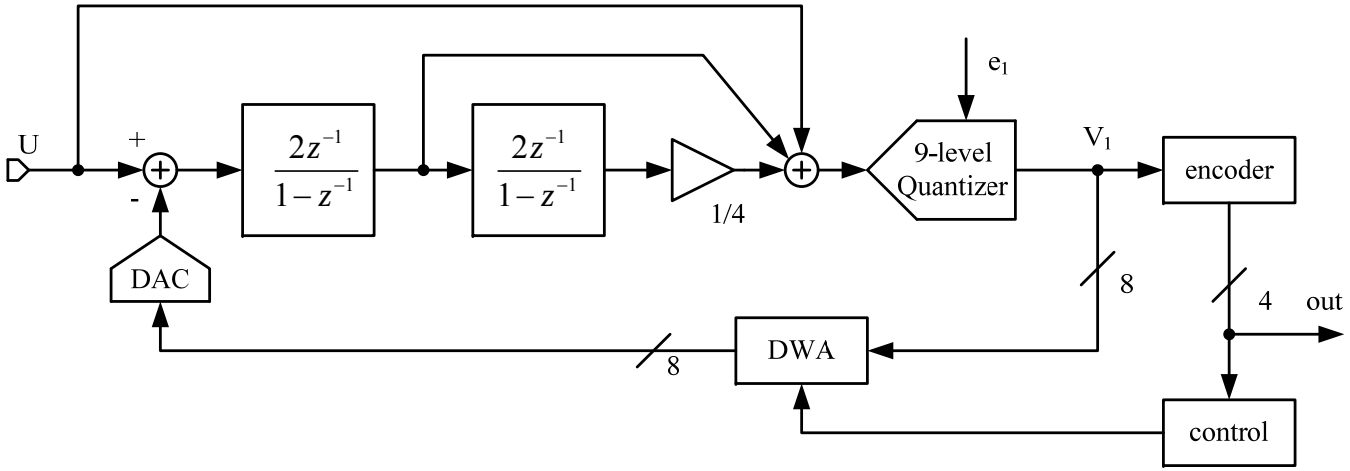
DWA implementation



- 5-level quantizer as an example

A ΔΣ modulator with multi-bit quantizer

- A well designed DWA only includes a shifter in the feedback path while the pointer calculation is outside the modulator loop [1]

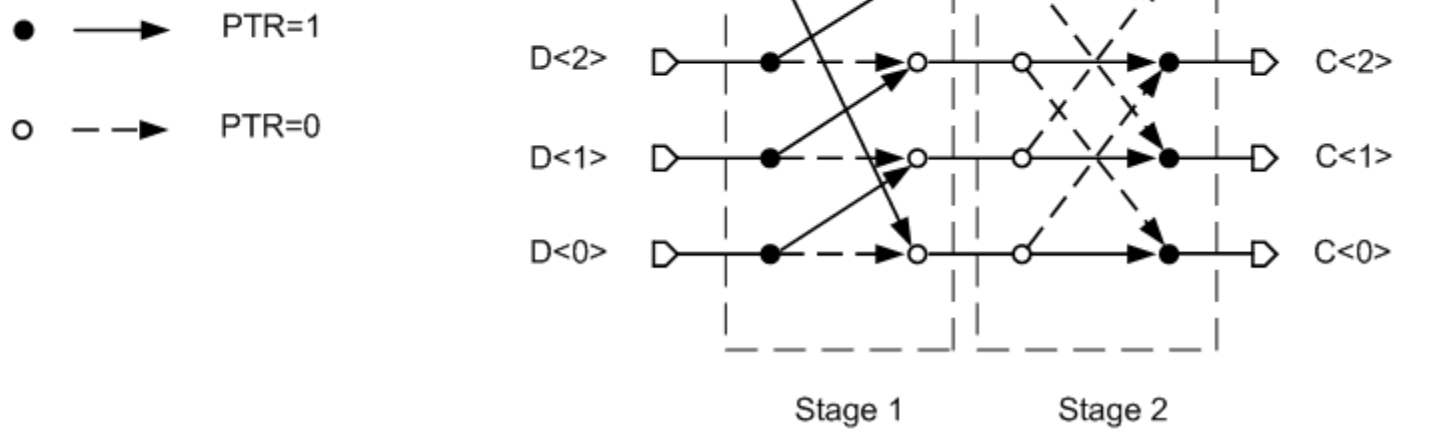


Pointer implementation

- Thermometer to binary code conversion
- Accumulator and register

Logarithmic shifter

- Transmission gate as a switch because it is able to pass both logic “0” and logic “1”



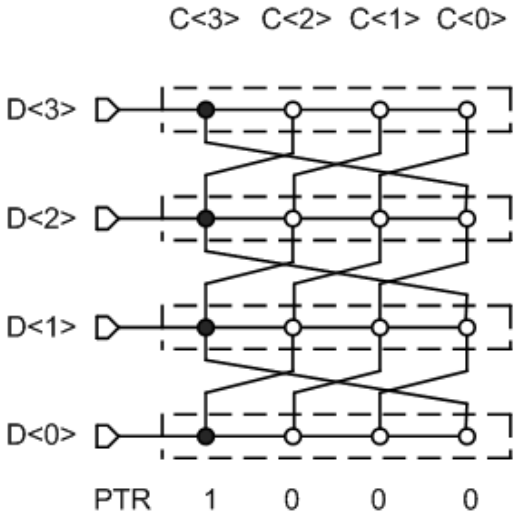
Logarithmic shifter

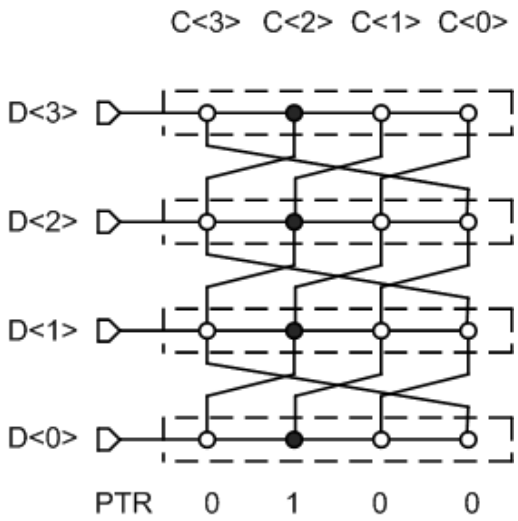
- Multi-stage design
- Speed is only moderate, but the total number of switches can be kept fairly small
- Total number of switches: $2*(N-1)*\log_2(N-1)$ where N is the number of quantizer levels
- Pointer is directly generated through an accumulator

Barrel shifter

- One stage design, so it is faster
- The number of switches $(N-1)^2$ grows rapidly with higher number of bits in the DAC
- Pointer needs to be decoded

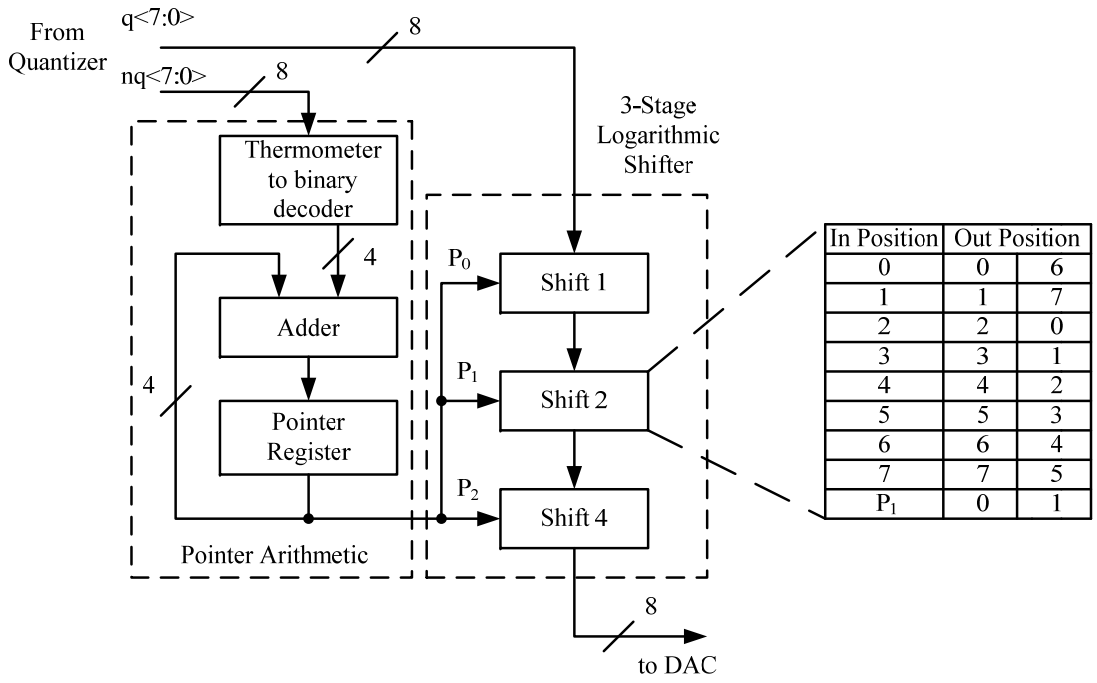
PTR	1000	0100	0010	0001
C<3>	D<3>	D<0>	D<1>	D<2>
C<2>	D<2>	D<3>	D<0>	D<1>
C<1>	D<1>	D<2>	D<3>	D<0>
C<0>	D<0>	D<1>	D<2>	D<3>





DWA implementation

- Overall circuit realization for a DWA using logarithmic shifter (9-level quantizer)



In Position	Out Position	
0	0	6
1	1	7
2	2	0
3	3	1
4	4	2
5	5	3
6	6	4
7	7	5
P_1	0	1

Other DWA implementations

- Bi-DWA [2]
- Pseudo-DWA [3]
- Partition-DWA [4]
- DWA can be performed already in the quantizer to completely eliminate the delay in the modulator feedback path [5]

References

1. M. Miller et al., “A Multibit Sigma-Delta AD for Multimode Receivers,” *IEEE J. Solid-State Circuits*, vol. 38, pp. 475-482, Mar. 2003.
2. I. Fujimori et al., “A 90dB SNR 2.5-MHz output rate ADC using cascaded multibit delta-sigma modulation at 8× oversampling ratio,” *IEEE J. Solid-State Circuits*, vol. 35, pp. 1820-1827, Dec. 2000.
3. A. A. Hamoui, and K. Martin, “High-order multi-bit modulators and pseudo data-weighted-averaging in low-oversampling ΔΣ ADCs for broad-band applications,” *IEEE T. Circuits and Systems*, vol. 51, pp. 72-85, Jan. 2004.
4. K. Vleugels et al., “A 2.5-V Sigma-Delta Modulator for Broadband Communications Applications,” *IEEE J. Solid-State Circuits*, vol. 36, pp. 1887-1899, Dec. 2001.
5. L. Dorrer et al., “10-Bit, 3 mW Continuous-Time Delta-Sigma ADC for UMTS in a 0.12μm CMOS Process,” in Proc. Eur. Solid-State Circuits Conf. (ESSCIRC), Lisbon, Portugal, Sept. 2003.