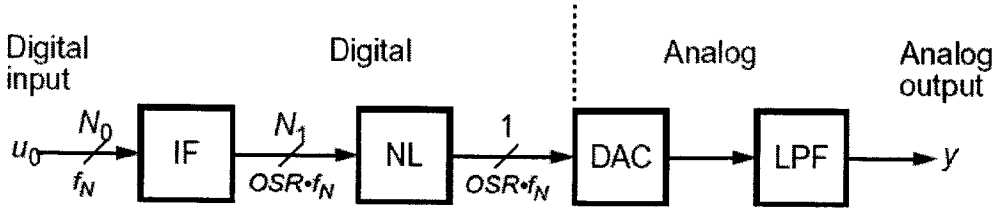
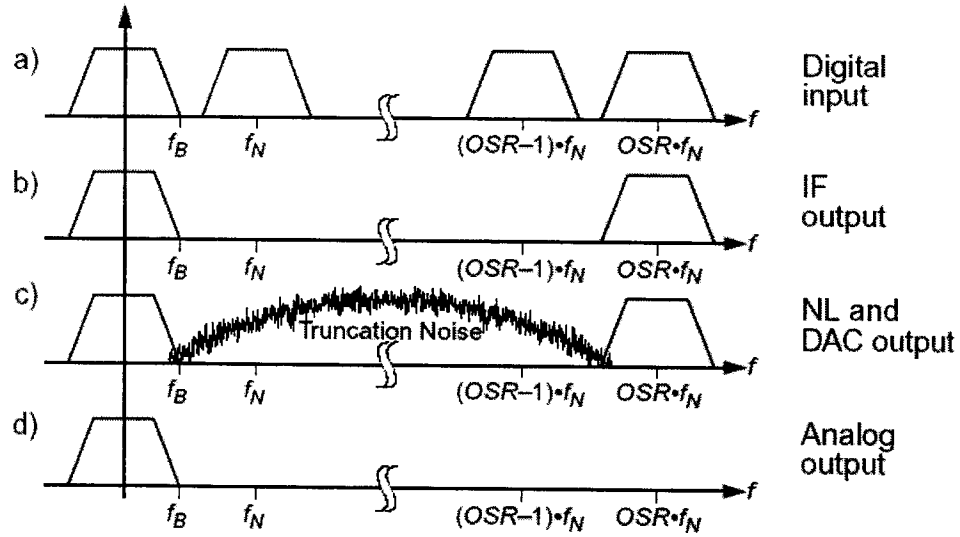
ΔΣ DAC STRUCTURE



IF: Interpolation Filter
NL: Noise-shaping Loop
DAC: Digital-Analog Converter
LPF: Lowpass Filter

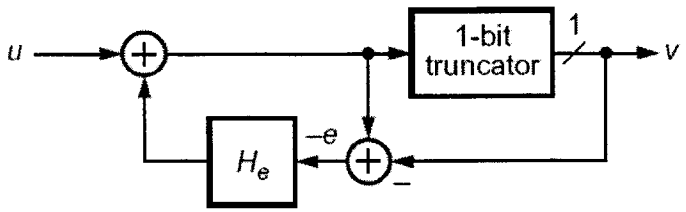
Block diagram of a ΔΣ DAC.

Single-bit DAC can be linear. For a few bits (2~4), DEM can be used



Signal and noise spectra in a ΔΣ DAC.

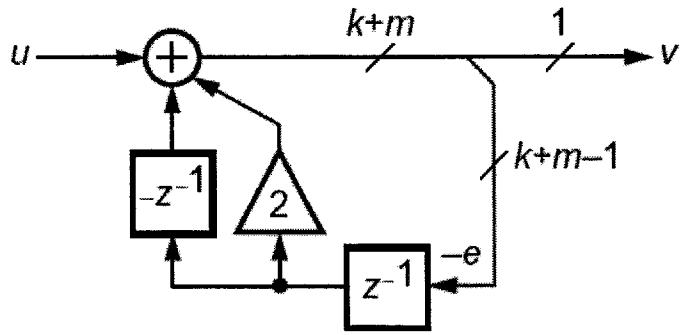
ERROR FEEDBACK ARCHITECTURE



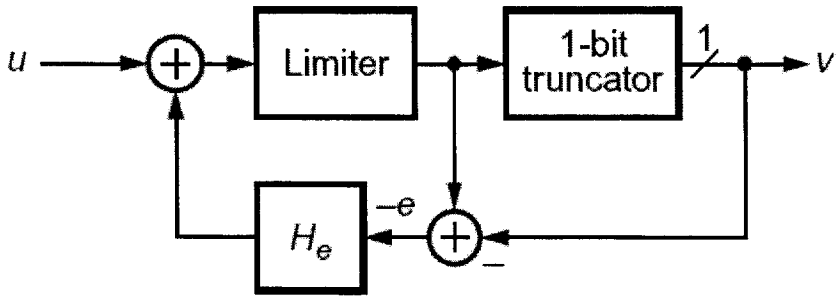
Error feedback structure.

$$V(z) = U(z) + [1 - H_e(z)]E(z)$$

$$H_e(z) = 1 - (1 - z^{-1})^2 = z^{-1}(2 - z^{-1})$$



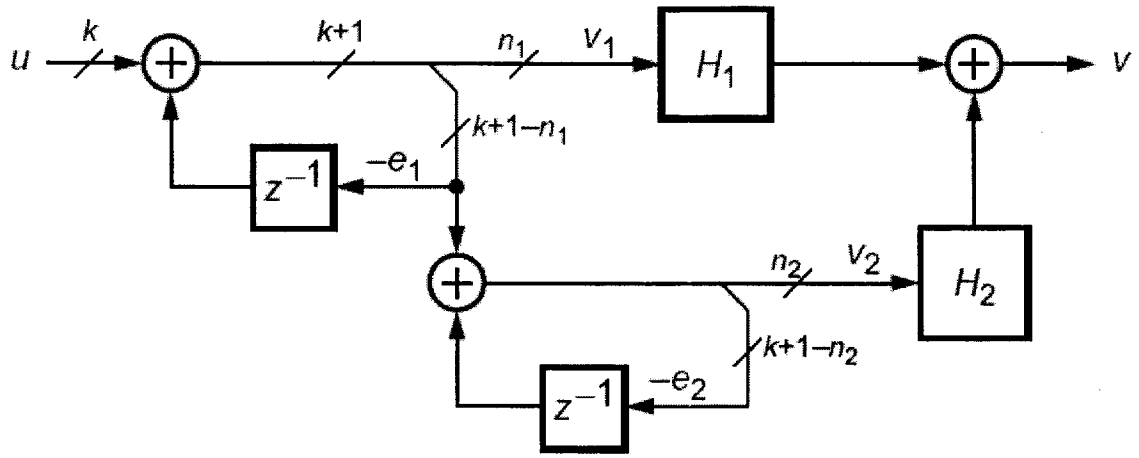
Second-order error-feedback noise-shaping loop.



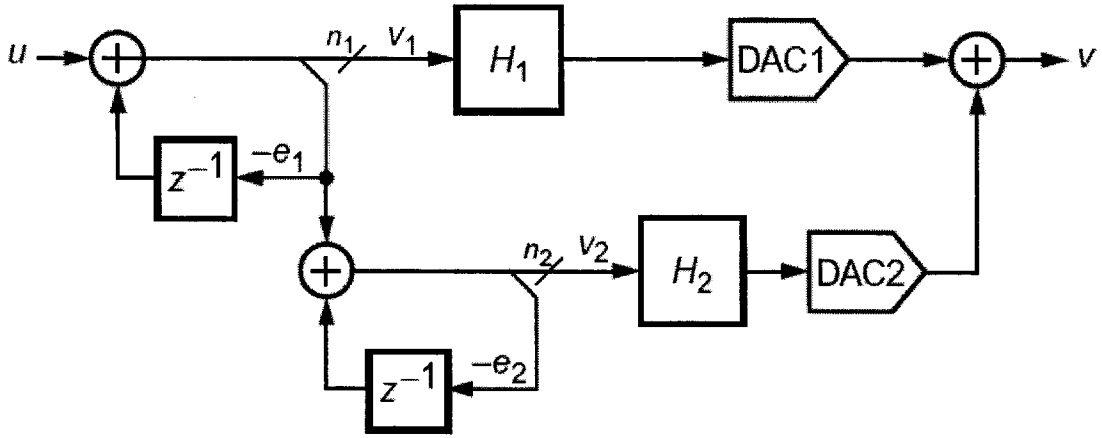
Error feedback with limiter.

Also, all ΔΣ configurations can be used

CASCADE DACs

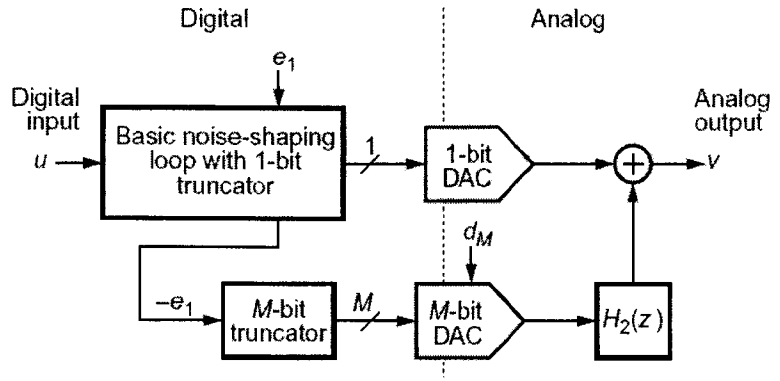


Cascade structure for a second-order noise-shaping loop.

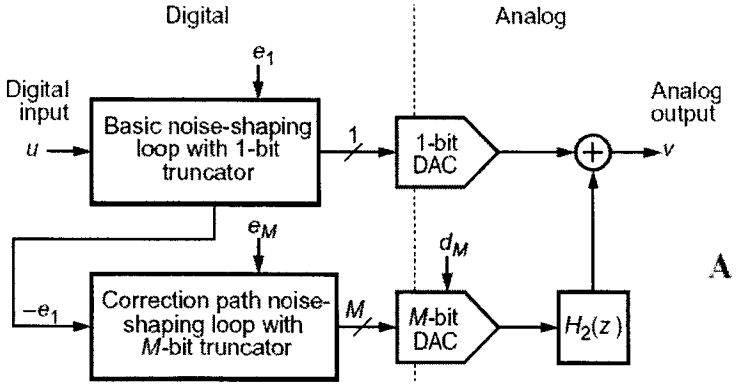


A cascade DAC using analog recombination.

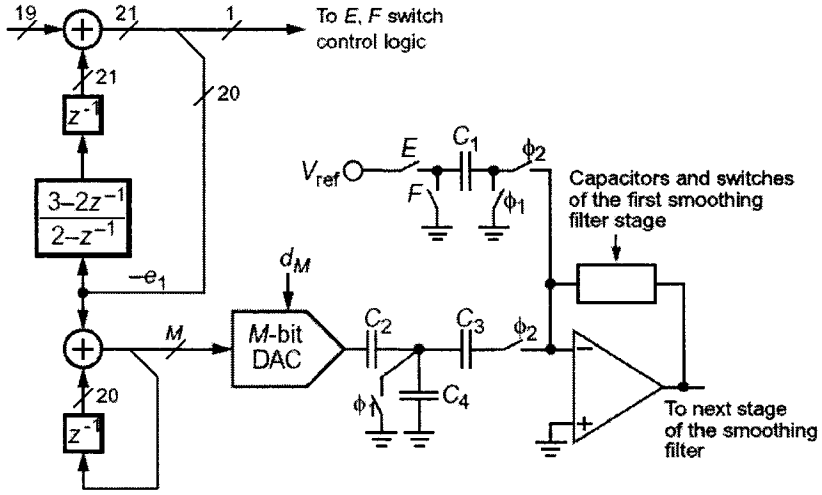
DUAL TRUNCATION DACs



A dual-truncation DAC system.

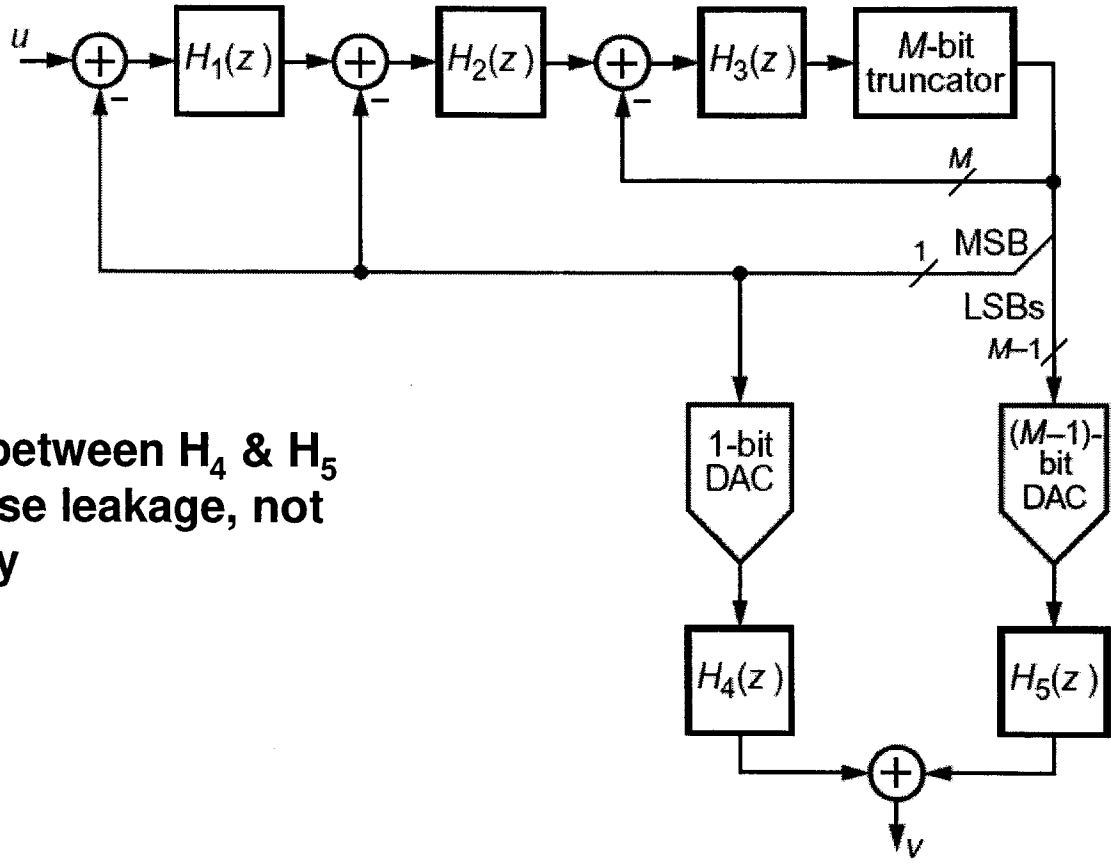


A dual-truncation MASH structure.



A third-order dual-truncation MASH noise-shaping stage.

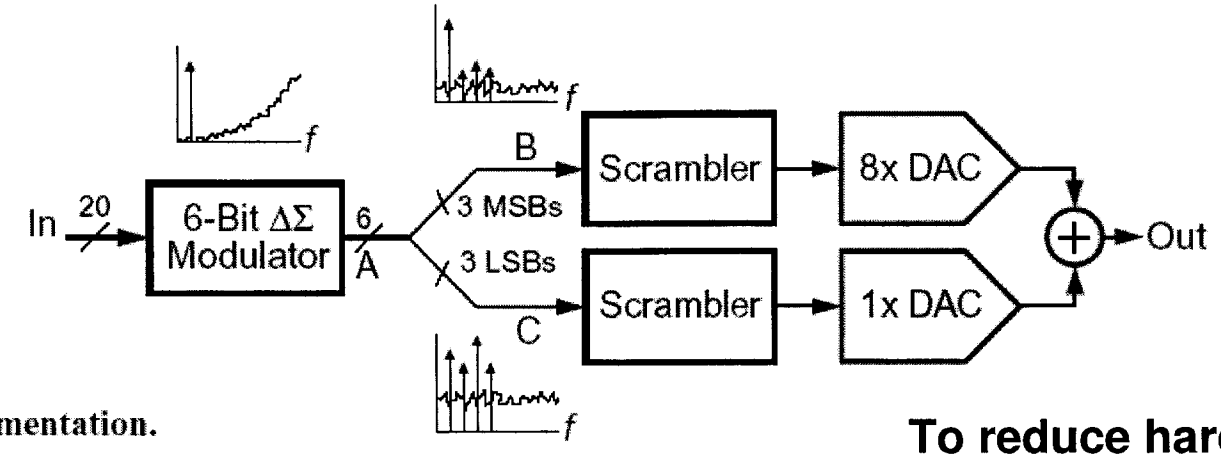
HARAPETIAN'S SCHEME



Mismatch between H_4 & H_5 causes noise leakage, not nonlinearity

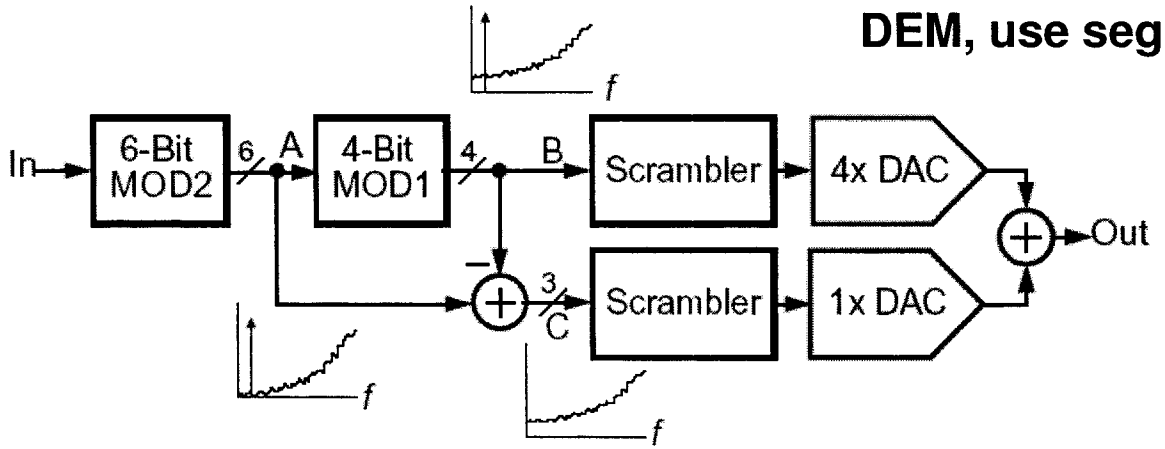
A single-stage dual-truncation D/A loop.

SEGMENTED DACs



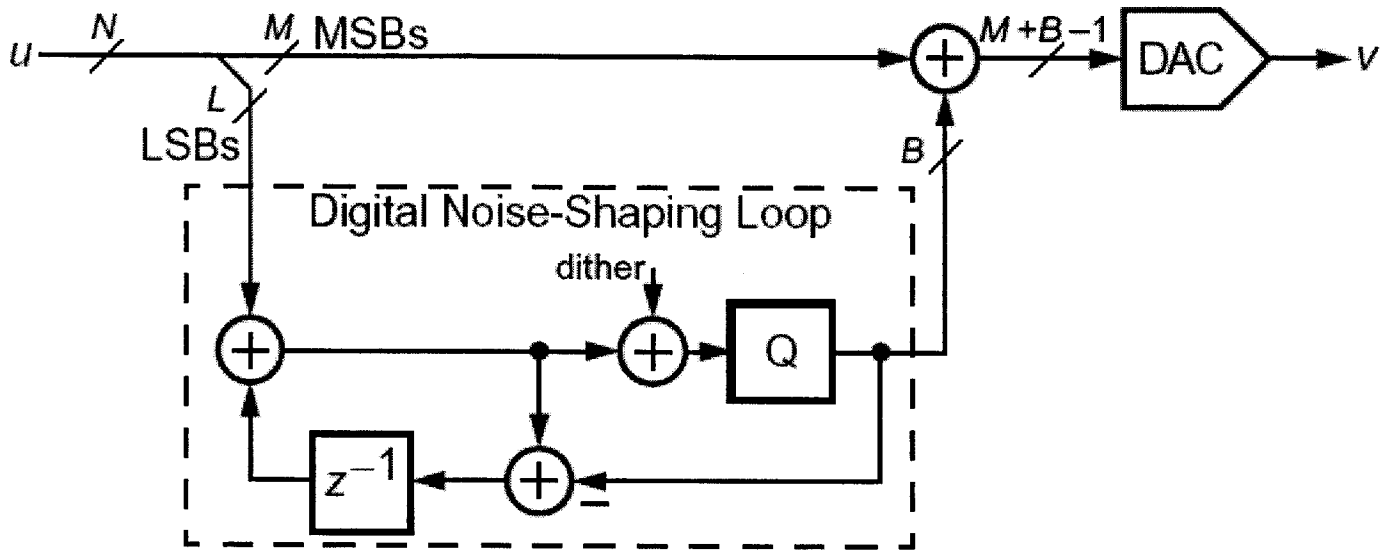
Segmentation.

To reduce hardware needed in the DAC and the DEM, use segmentation



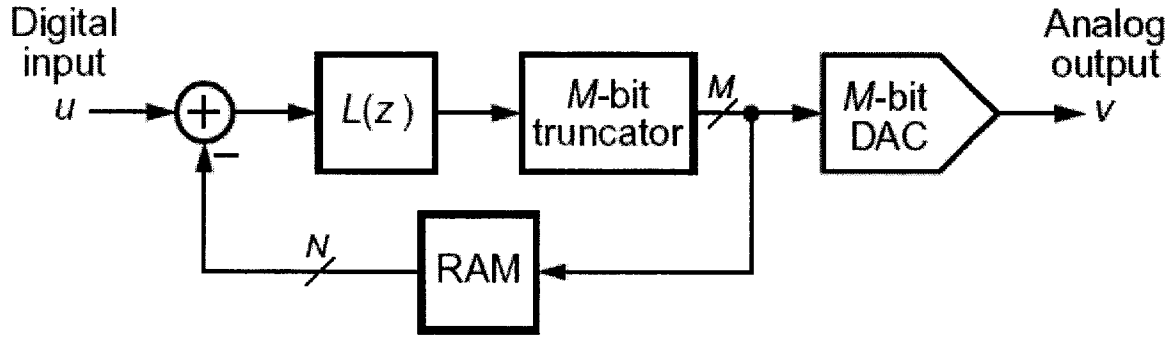
Noise-shaped segmentation.

ANOTHER SEGMENTATION SCHEME

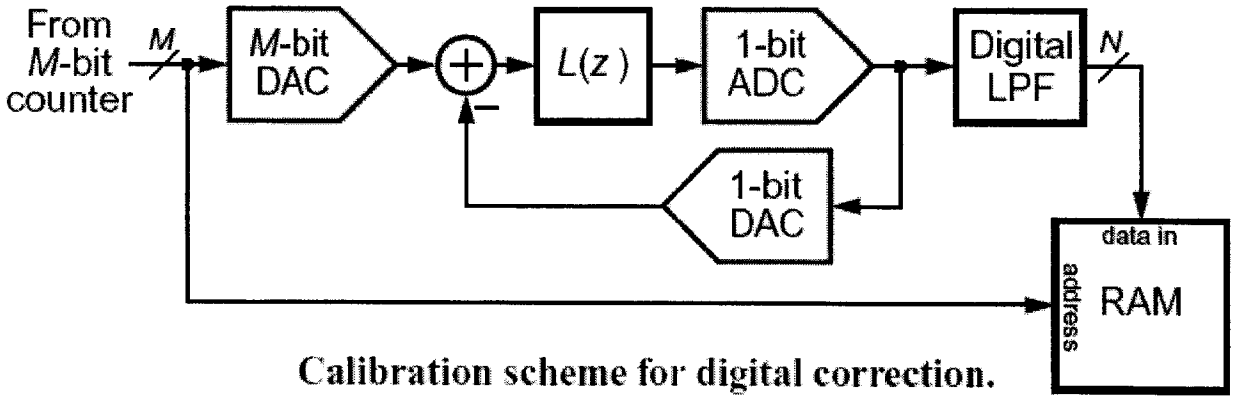


A hardware-reduced first-order modulator with dither.

A POWER-UP CORRECTION METHOD



A digitally-corrected *M*-bit DAC.



Calibration scheme for digital correction.

COMPARISON OF SINGLE- AND MULTI-BIT ΣΔ DACS

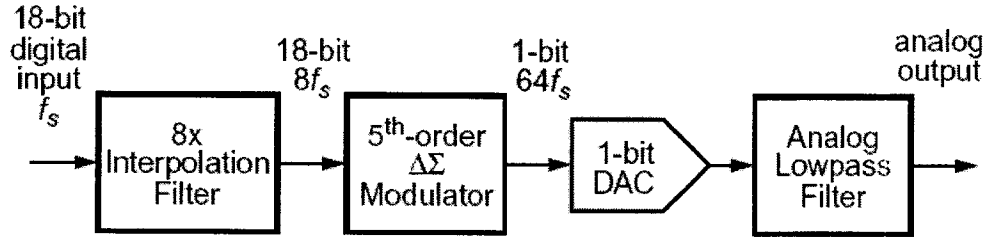
Single-bit truncation: Much simpler internal DAC structure can be used, without the need for thermometer coding, unit elements and digital mismatch-shaping logic.

Multi-bit truncation: Several advantages can be obtained, including

1. Simpler digital noise-shaping loop, since more aggressive NTF may be used, and since the truncation noise is reduced by at least $N-1$ bits.
2. Less (or no) dithering, since tones are less likely to be generated, and since typically the amplitude of dithering is about 1/2 LSB, which is smaller in a multi-bit quantizer.
3. Much simpler analog smoothing filter, since the slewing and out-of-band noise in the DAC output are both reduced. Also, the sensitivity to clock jitter is reduced, due to the reduced step size in the DAC output signal.[†]

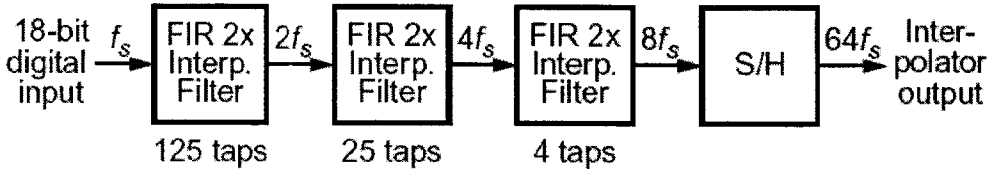
Generally, the advantages of multi-bit truncation outweigh those of single-bit truncation, and hence it is preferable to design ΔΣ DACs with multi-bit internal DACs.

AN EXAMPLE [3]

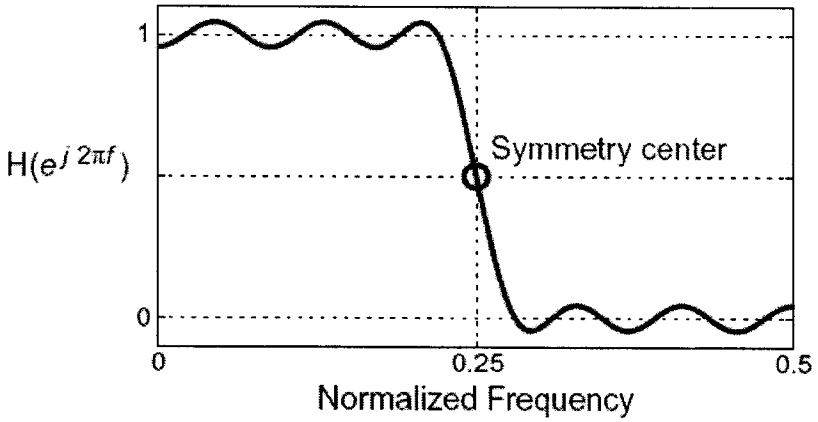


An 18-bit D/A converter architecture.

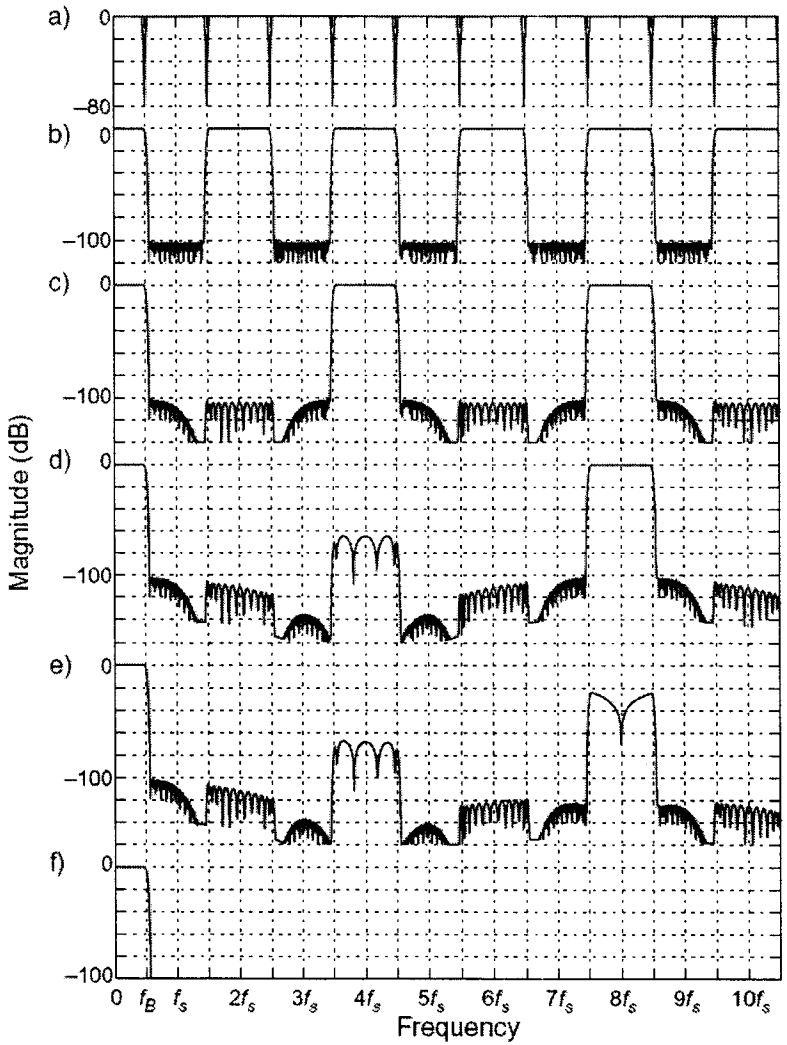
Interpolation filter architecture.



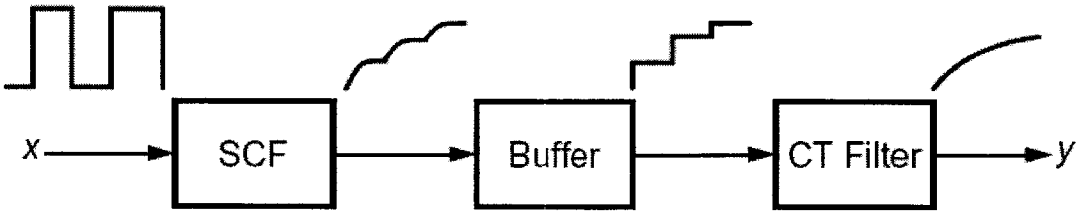
Frequency response of a half-band filter.



SPECTRA WITHIN $\Delta\Sigma$ DAC SYSTEM

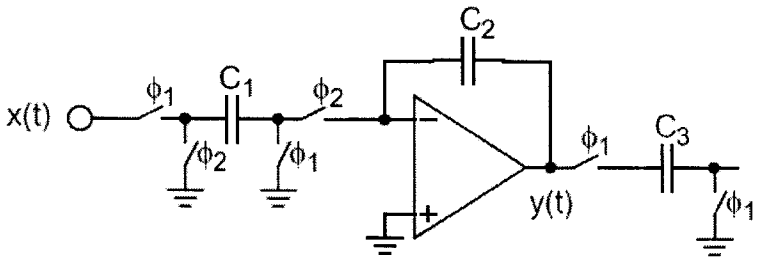


POST-FILTER DESIGN

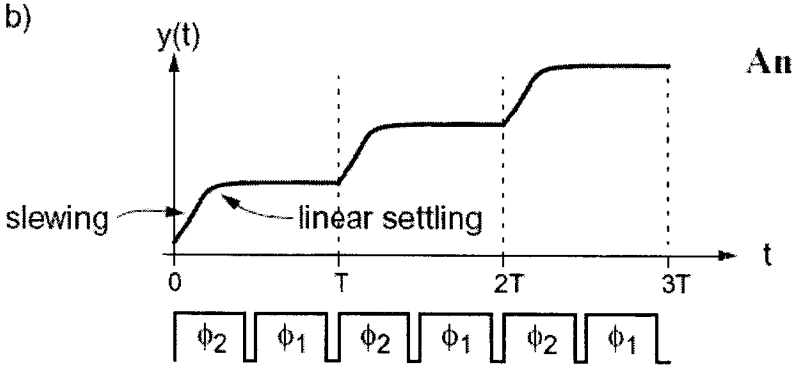


Post-filter for a 1-bit ΔΣ DAC and associated signals.

a)

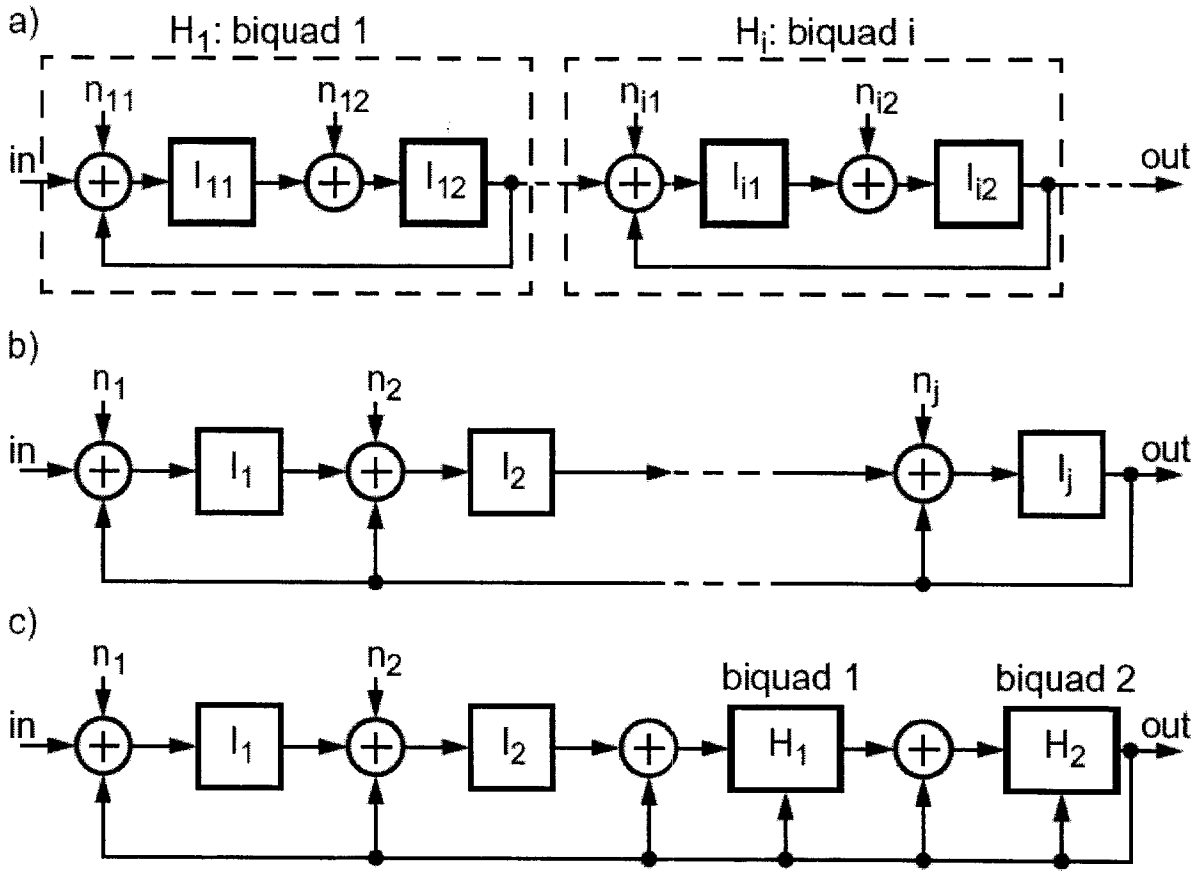


b)



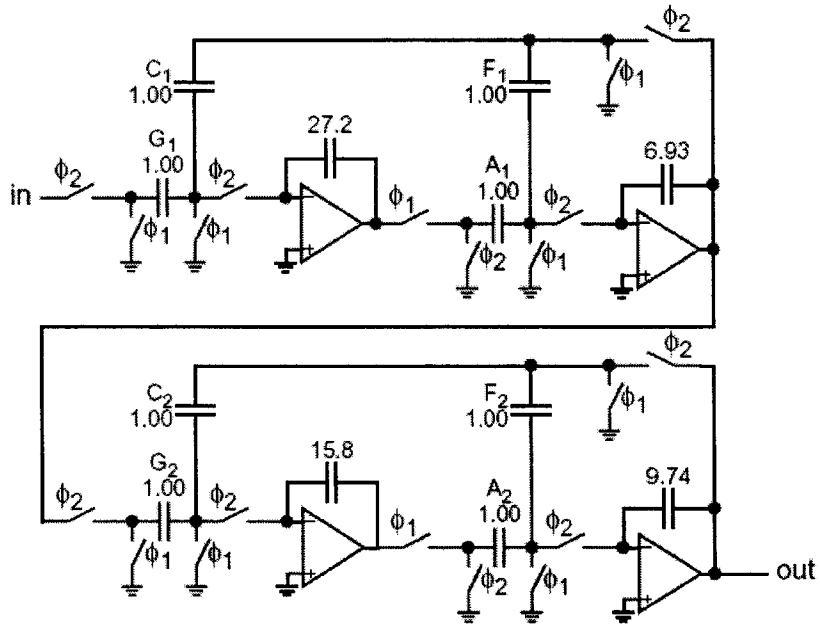
An SC integrator.

RECONSTRUCTION FILTER ARCHITECTURES

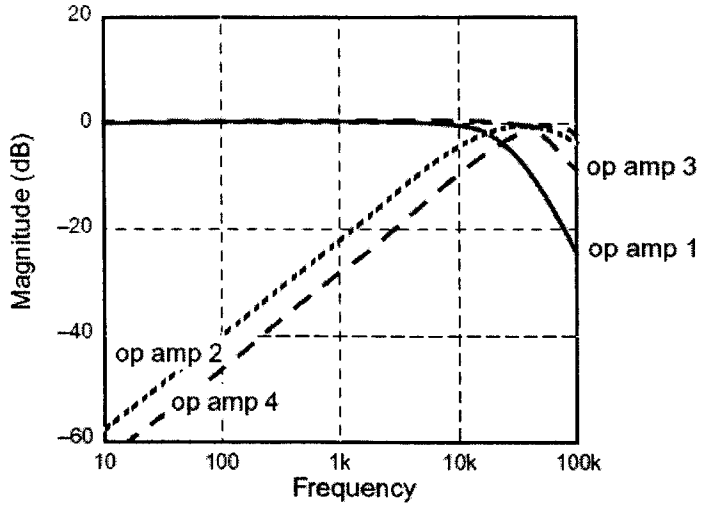


POST-FILTER EXAMPLES (1)

A 4th-order Bessel filter implemented with a cascade of biquads.

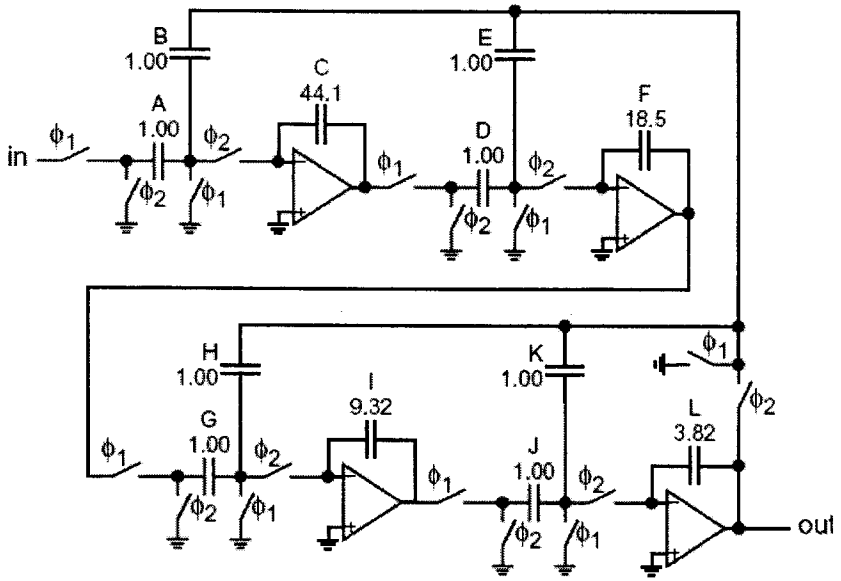


Noise gains from each op-amp input

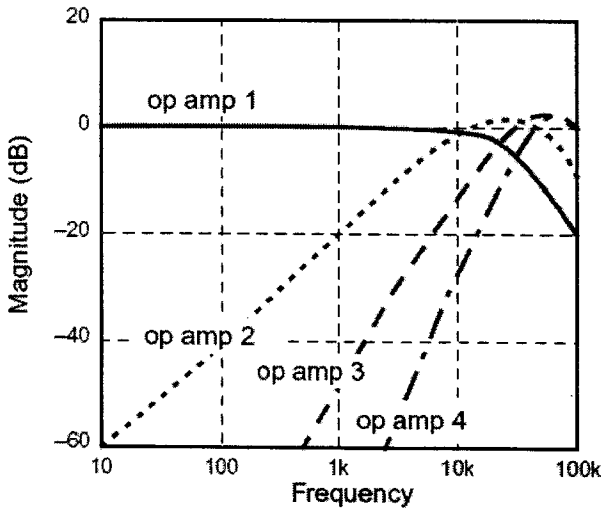


POST-FILTER EXAMPLES (2)

A 4th-order Bessel filter implemented with the inverse follow-the-leader topology.

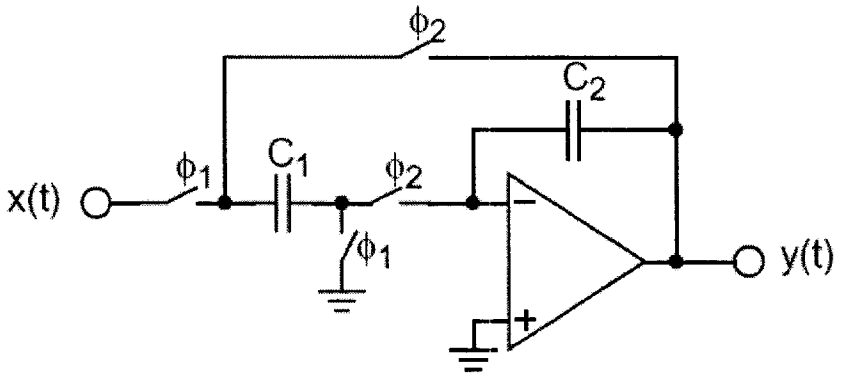


Noise gains from each op-amp input

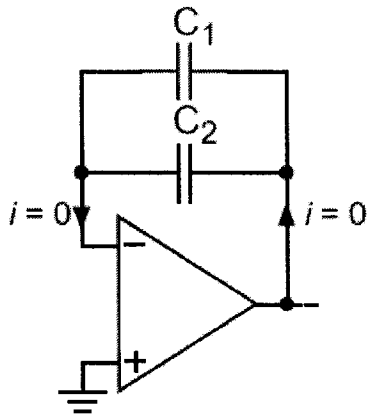


SC-CT BUFFER

a)

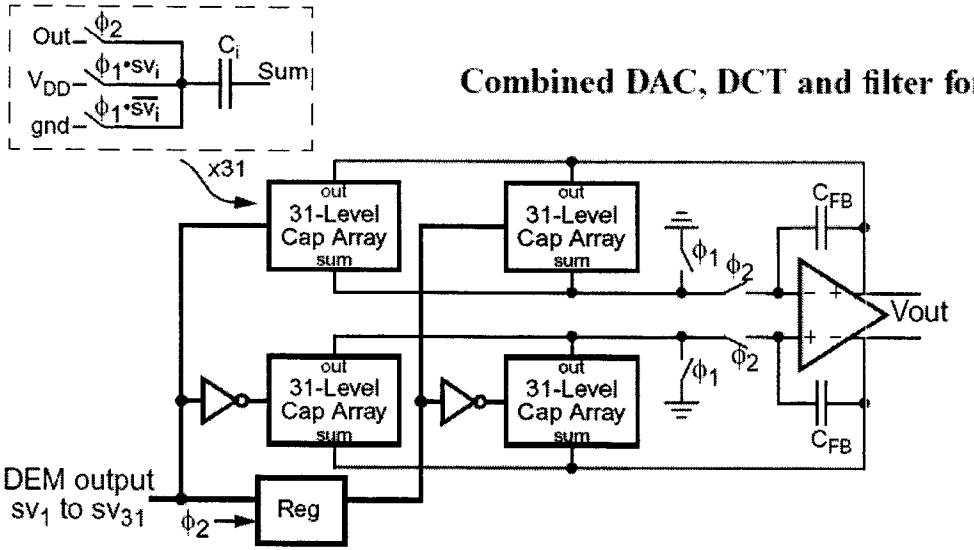


b)

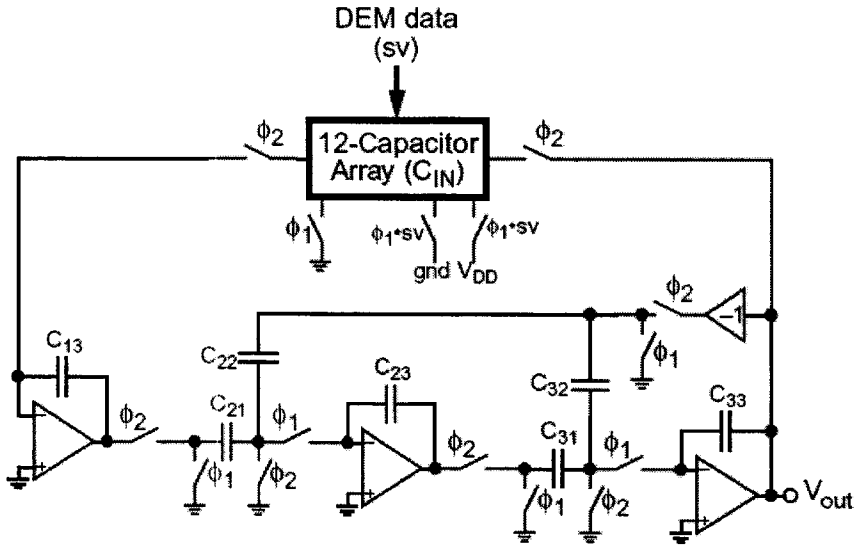


A direct-charge-transfer (DCT) stage.

DESIGN EXAMPLES



Combined DAC, DCT and filter for a multi-bit ΔΣ DAC [8].



Another ΔΣ DAC with merged DAC, DCT and SCF filter functions [15].

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[4] X. F. Xu and G. C. Temes, "The implementation of dual-truncation ΣΔ D/A converters," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 597-600, May 1992.

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[8] I. Fujimori, A. Nogi and T. Sugimoto, "A multibit Δ-Σ audio DAC with 120-dB dynamic range," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 1066-1073, August 2000.

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[12] M. Rebeschini and P. F. Ferguson, Jr., "Analog Circuit Design for ΔΣ DACs," in S. Norsworthy, R. Schreier and G.C. Temes, *Delta-Sigma Data Converters*, Sec. 12.2.3, IEEE Press, 1997.

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[14] See, e.g., R. Schaumann and M.E. Van Valkenburg, *Design of Analog Filters*, pp. 161-163, Oxford University Press, 2001.

[15] M. Annovazzi et al., "A low-power 98-dB multibit audio DAC in a standard 3.3-V 0.35-μm CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 825-834, July 2002.