Design Examples

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Catalog

1. MOD2

Specifications

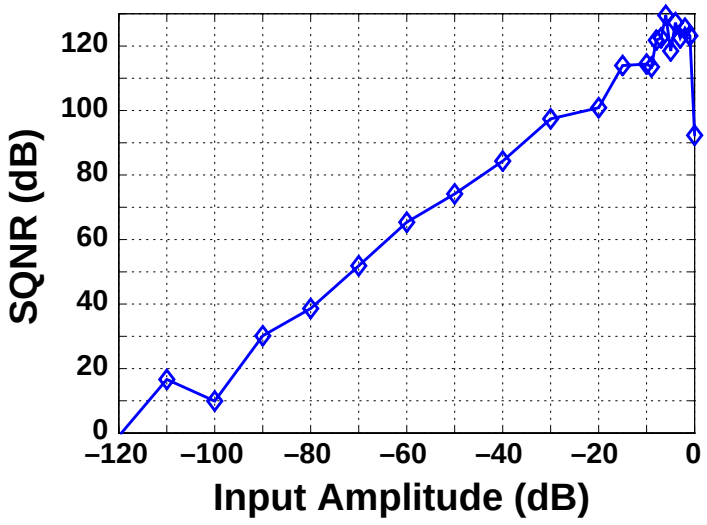
Parameter	Symbol	Value	Units
Bandwidth	f_B	~1	kHz
Sampling Frequency	f_S	1	MHz
Signal-to-Noise Ratio	SNR	100	dB
Supply Voltage	VDD	3	V

Assumptions

- **Single-bit switched-capacitor realization**
- **Input voltage range is 0-VDD (single-ended)**
  Reference voltage is VDD
  Op-amp swing is 2 V_{pp} (differential)

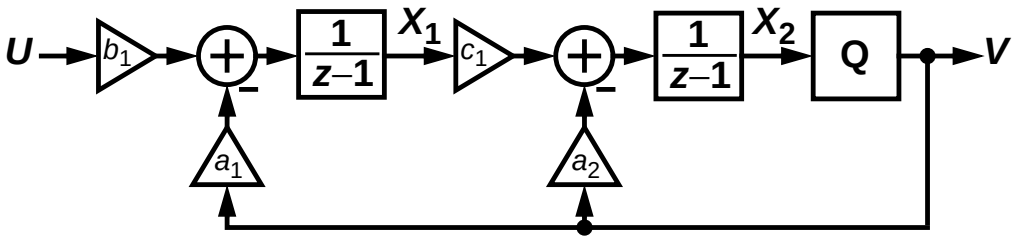
Toolbox Design

```
OSR = 500;
H = synthesizeNTF(2,OSR,0,2);
[snr amp] = simulateSNR(H,OSR);
plot(amp,snr,'bd',amp,snr,'b-');
```



- **Very high SQNR**
  ⇒ Quantization noise will be negligible.
- **Maximum input signal ≈ –1 dBFS**
  ⇒ Let's not worry about instability.

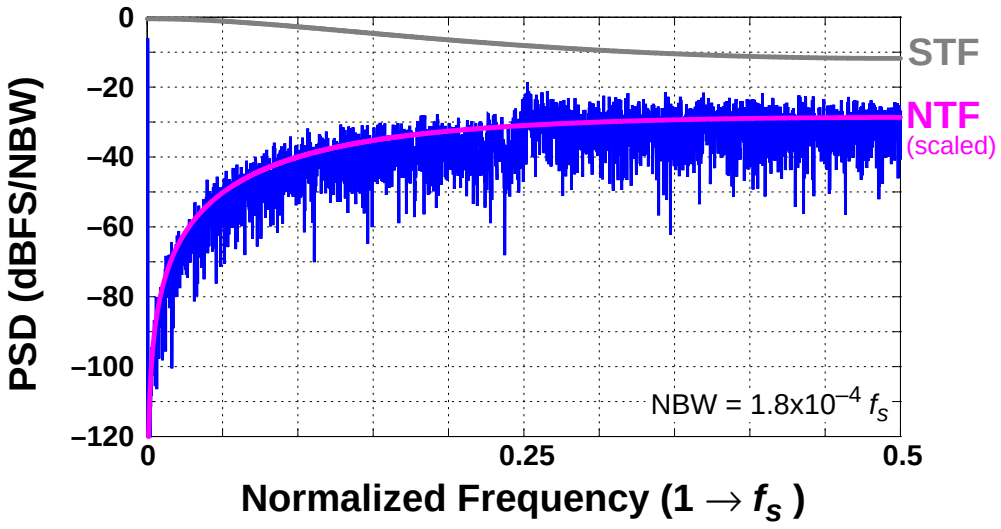
Block Diagram & DR Scaling




```
form = 'CIFB';
[a,g,b,c] = realizeNTF(H,form);
b(2:end) = 0;
ABCD = stuffABCD(a,g,b,c,form);
[ABCDs umax] = scaleABCD(ABCD);
[a,g,b,c] = mapABCD(ABCDs,form);
```

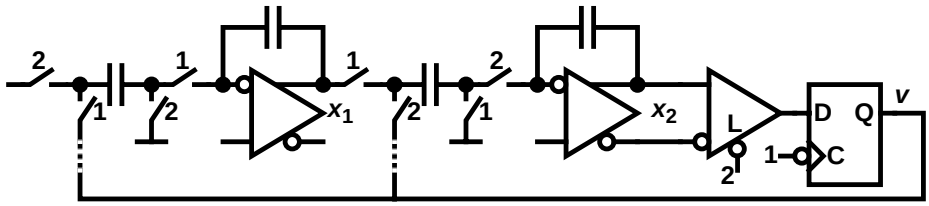
- **Code yields a = [0.27, 0.24], b = [0.27], c = [0.34 5.1], u_{max} = 0.9**
  - **Quantize to $a_1 = b_1 = a_2 = 1/4$, $c_1 = 1/3$ for convenience.**

Simulated Spectrum



- **Coefficient change has negligible performance impact**
  - **Peak SQNR = 115 dB, $\|H\|_\infty$ = 2.2.**

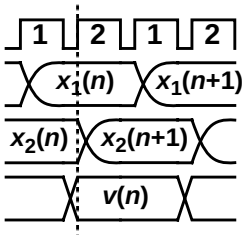
Simplified Schematic



Difference Equations

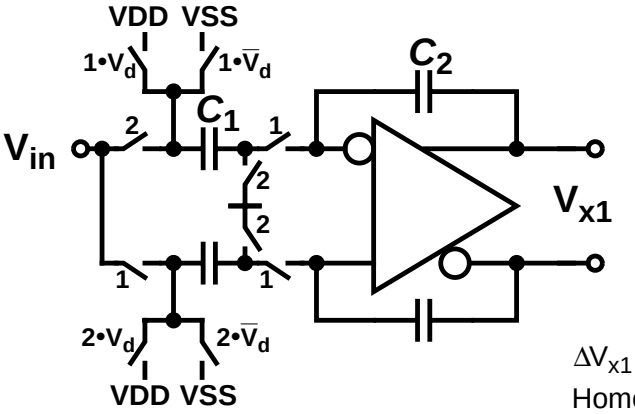
$$x_1(n+1) = x_1(n) + b_1 u(n) - a_1 v(n)$$
$$x_2(n+1) = x_2(n) + c_1 x_1(n) - a_2 v(n)$$
$$v(n) = Q(x_2(n))$$

Timing



- **Verify that the circuit follows the difference equations. Check the quantizer and feedback timing carefully!**

First Integrator



0, 1

$\Delta V_{x1} = 2C_1/C_2 \cdot (V_{in} - V_{DD} \cdot v_d)$

Homework: Verify timing & polarity

- **Want input (full-scale) range = [0,3] V and want op-amp swing = [–1,+1] $V_{differential}$**

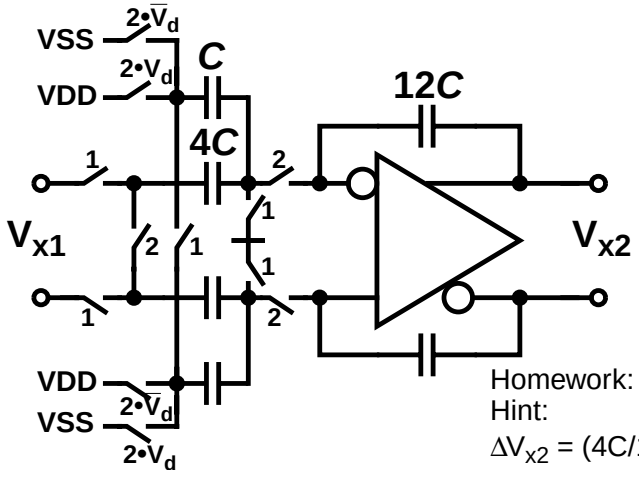
  $x_1 = V_{x1}/1\text{ V}$, $u = (V_{in} - 1.5\text{ V})/1.5\text{ V}$

$$\Rightarrow C_1/C_2 = b_1/3 = 1/12$$

Absolute Capacitor Values

- **Absolute capacitor values are determined by thermal noise considerations**
  - **Capacitor ratios are set by the desired dynamics.**
- **For example, assume noise is purely *kT*/*C* noise**
  - **i.e. device noise is negligible.**
- **Since thermal noise is white, we get a factor of OSR reduction in the in-band noise**
  - **i.e.** $v_n^2 = \frac{1}{OSR} \bullet \frac{kT}{C_1}$
- $v_n = 10\ \mu V_{rms} \Rightarrow C_1 = 83\ fF \Rightarrow C_2 = 1\ pF$
  - **These capacitor values are quite reasonable!**
  - C_2 **gets smaller if the output swing of the op-amp is increased.**

Second Integrator

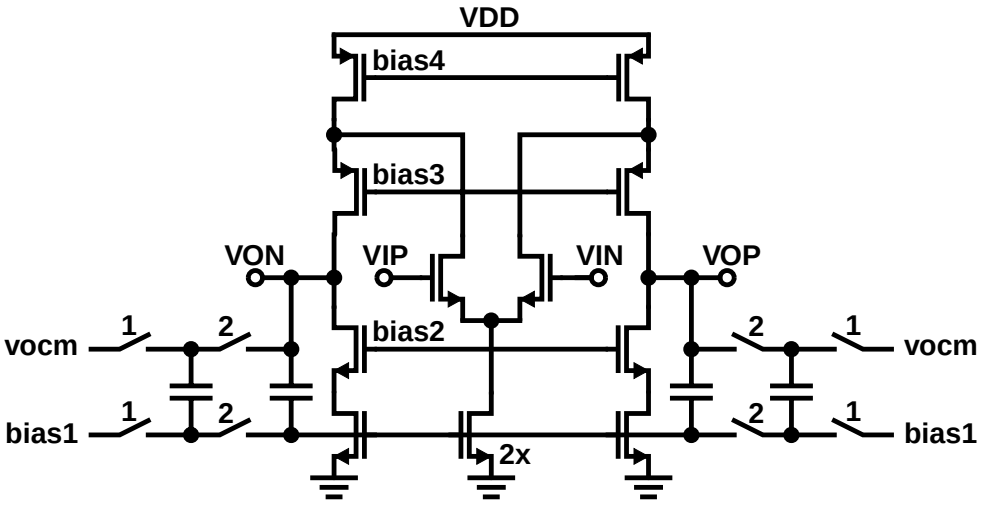


Homework: Verify capacitor ratios
Hint:
$\Delta V_{x2} = (4C/12C) \cdot V_{x1} - (C/12C)\ V_{DD} \cdot v)$ ± 1

- **In-band noise of second integrator is greatly attenuated**
  - **By a factor of** $\frac{(OSR)^3}{12^2} \approx 10^6$ **(approximately).**

$\Rightarrow$ **Capacitor sizes dictated by charge injection errors and desired ratio accuracy**

Building Block– Op Amp



- **Folded-cascode op-amp with switched-capacitor common-mode feedback**

Op-Amp Specifications

- **50% of $T/2$ = 0.25 μs; $Q_{max} = C_1 VDD$ = 0.25 pC $\Rightarrow I_{slew}$ = 1 μA is sufficient**
- **$T/2 = 10\tau$; $\tau = C_1/g_m$; C_1 = 0.1 pF $\Rightarrow g_m$ = 2 μA/V**

  Power consumption can be very low!

- **As a rule of thumb, $A_{min} \approx OSR$ for negligible SQNR reduction**

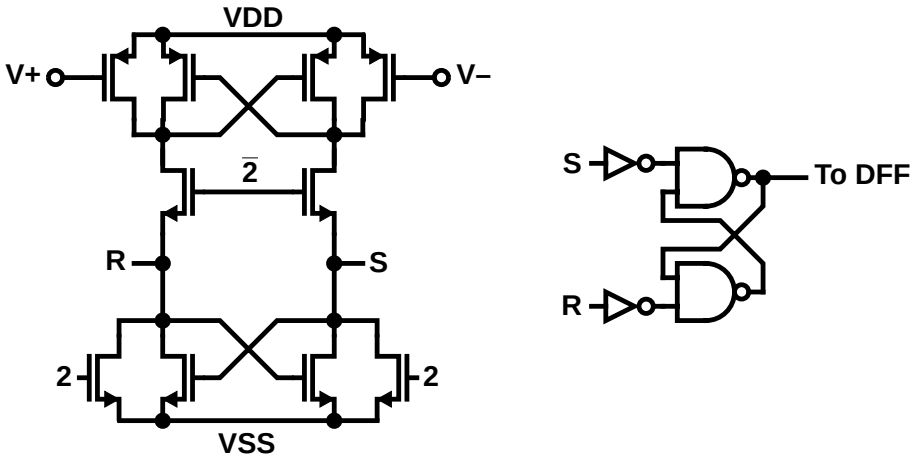
  Assumes that the op amps are linear and that the integrator gain factors are close to 1.

  SQNR margin can be traded for reduced op-amp gain requirements.

- **In this implementation, the integrator gain factors are 1/3 and 1/12, and the gain requirements are relaxed**

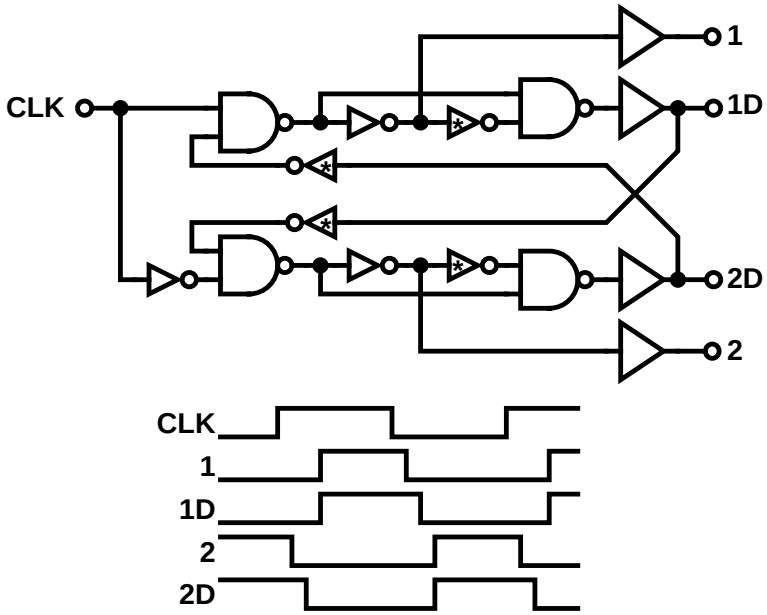
  For example, A = 40 dB is sufficient for 110 dB SQNR and the width of the deadband around 0 V is only 4 μV if A = 40 dB.

Building Block– Latched Comparator



- **Falling phase 2 initiates regenerative action**
  S and R connected to a Set/Reset latch

Building Block– Clock Generator



* = Delay Control

2. MOD5

Specifications

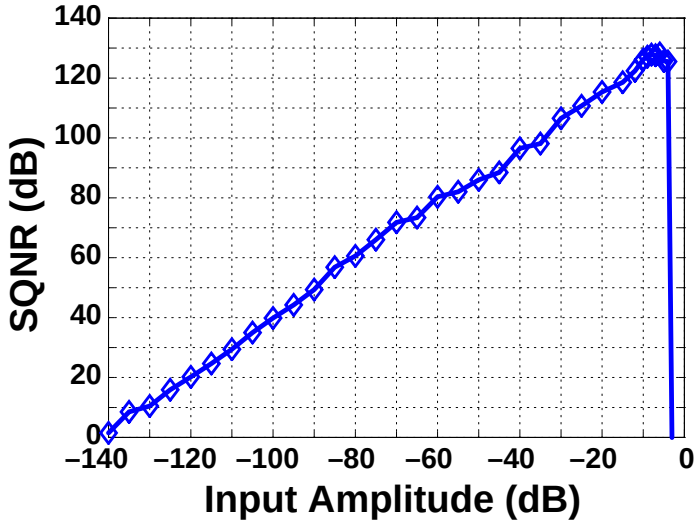
Parameter	Symbol	Value	Units
Signal Bandwidth	f_B	50	kHz
Sampling Frequency	f_S	8	MHz
Signal-to-Noise Ratio	SNR	110	dB
Supply Voltage	VDD	3	V

Assumptions

- Single-bit switched-capacitor realization
- Input voltage range is ±2 V (differential)
- Reference voltage is 2 V (differential) and Op amp swing is 4 V_{pp} (differential)

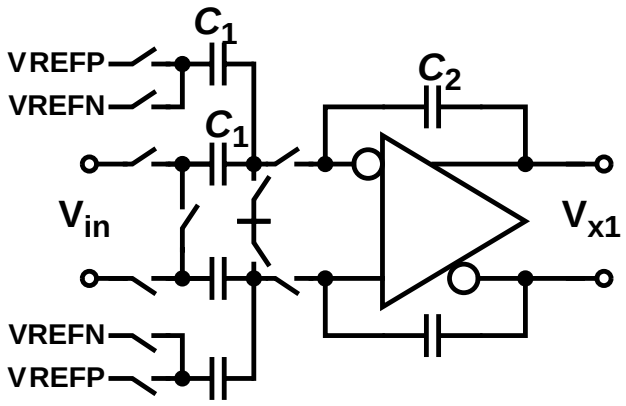
Toolbox Design

```
OSR = 8e6/(2*50e3);      % OSR = 80
H = synthesizeNTF(5,OSR,1,1.5);
amp = [-140:5:-15 -12 -10:0];
snr = simulateSNR(H,OSR,amp);
plot(amp,snr,'bd',amp,snr,'b-');
```



- Very high peak SQNR
  ⇒ Quantization noise will be negligible.
- Maximum input signal ≈ –4 dBFS
  ⇒ Scale such that input range is 50% of full-scale.

First Integrator



- **Input-referred differential noise power is $P_n = 8\frac{kT}{C_1}$**
  Peak signal power is $P_s = (2\text{ V})^2/2 = 2\text{ V}^2$
- **110 dB SNR requires $C_1 = \frac{8kT \bullet SNR}{OSR \bullet P_s} = 21$ pF**
  This is a big capacitor!

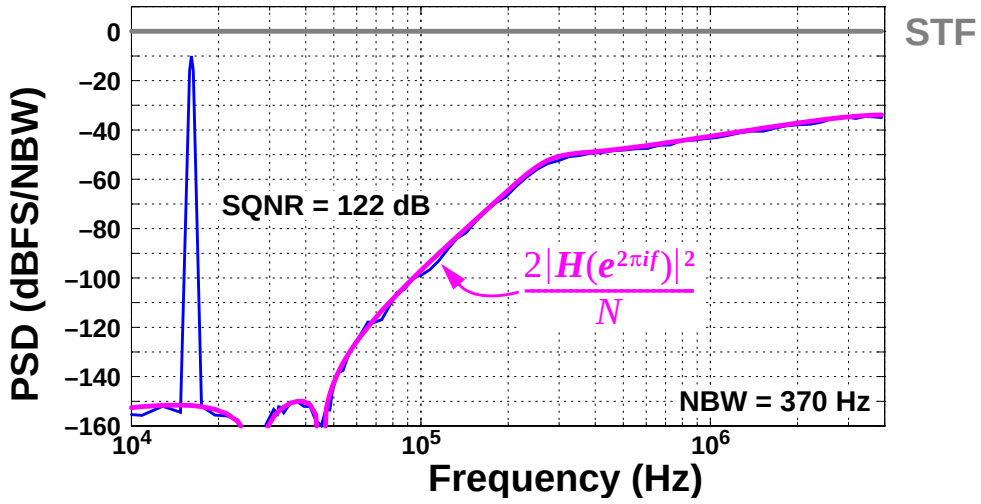
Dynamic Range Scaling & Topology Selection

```
form = 'CRFB';      % or 'CRFF'
[a,g,b,c] = realizeNTF(H,form);
b(2:end) = 0;       % for CRFB only
ABCD = stuffABCD(a,g,b,c,form);
[ABCDs umax] = scaleABCD(ABCD);
[a,g,b,c] = mapABCD(ABCDs,form);
```

- **`form = 'CRFB'` yields $b_1 = 0.1$, i.e. $C_2 = 10C_1$!**
  The integrating capacitor is VERY large!
- **`form = 'CRFF'` yields $b_1 = 0.39$, i.e. $C_2 = 2.5C_1$**
  The integrating capacitor is still large, but is more reasonable.

Simulated Spectrum

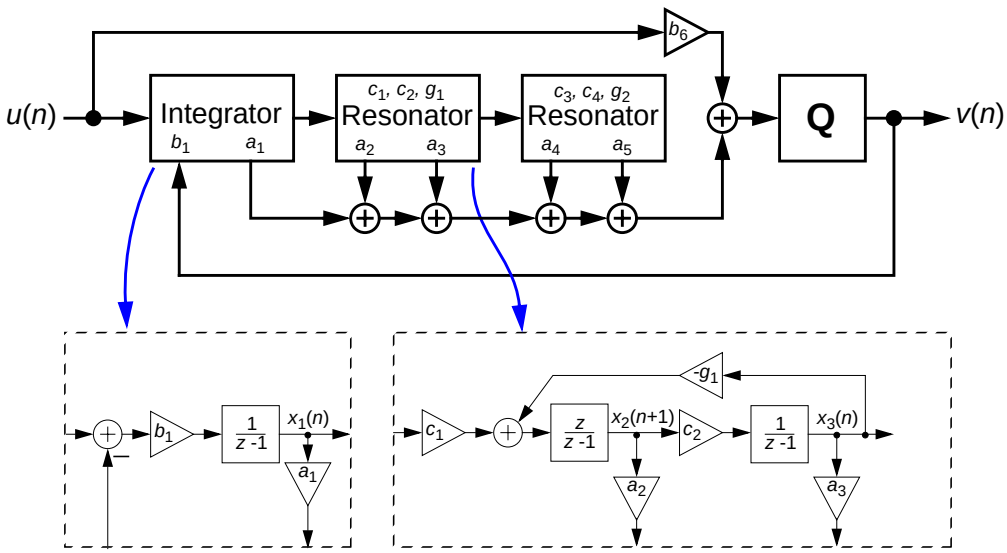
–10 dBFS input



- **Used *k* derived from simulation to calculate "true" NTF**

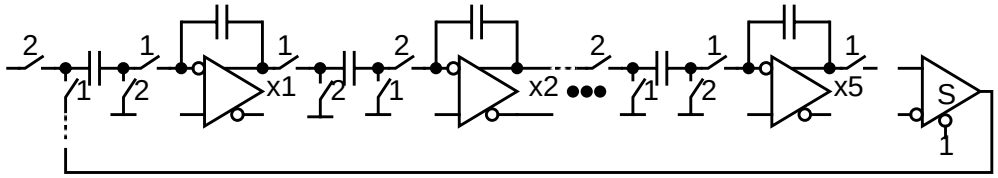
  Need to set $b_6 = 1/k$ to maintain unity STF.

Block Diagram



- **Summation is usually performed by a single passive switched-capacitor network**

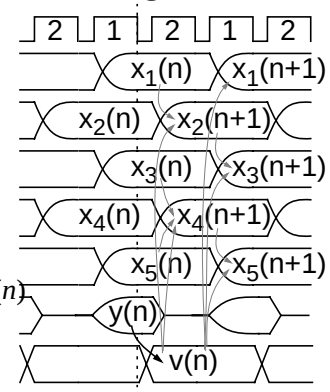
Timing Check



Desired Difference Equations

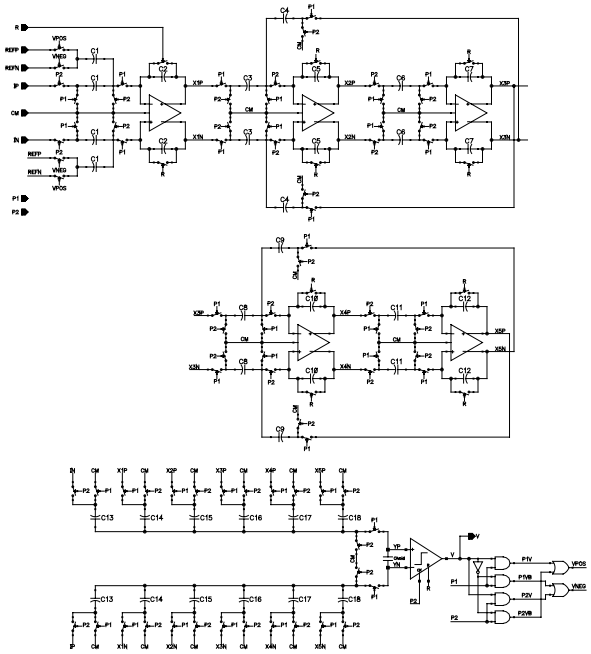
$$x_1(n+1) = x_1(n) + b_1u(n) - c_1v(n)$$
$$x_2(n+1) = c_2x_1(n) + x_2(n) - g_1x_3(n)$$
$$x_3(n+1) = c_3x_2(n+1) + x_3(n)$$
$$x_4(n+1) = c_4x_3(n) + x_4(n) - g_2x_5(n)$$
$$x_5(n+1) = c_5x_4(n+1) + x_5(n)$$
$$y(n) = a_1x_1(n) + a_2x_2(n+1) + a_3x_3(n) + a_4x_4(n+1) + a_5x_5(n) + b_6u(n)$$
$$y_a(n) = (a_1 + a_2c_2)x_1(n) + a_2x_2(n) + (a_3 - a_2g_1 + a_4c_4)x_3(n) + a_4x_4(n) + (a_5 - a_4g_2)x_5(n) + b_6u(n-1)$$
$$v(n) = Q[y(n)]$$

Timing

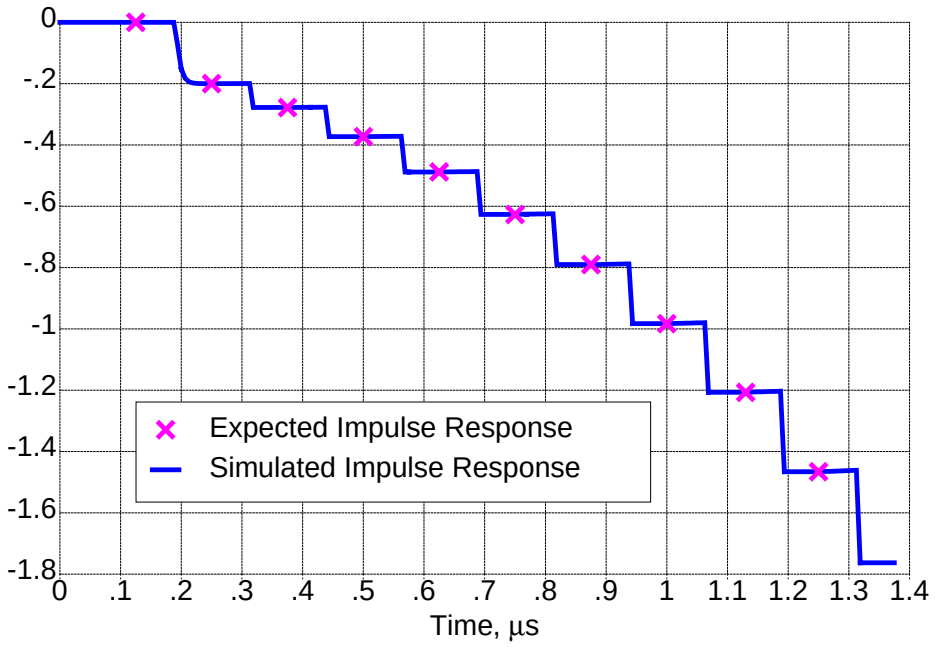


$$[y_a = y + b_6(u(n-1) - u(n)) \Rightarrow STF_a(z) = STF(z) - (1 - z^{-1})NTF(z)]$$

Behavioral Schematic



Impulse Response Verification



Potential Improvements

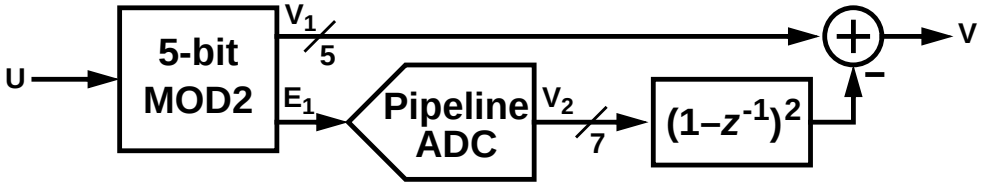
- **Clock faster**
  - **Reduces modulator order.**
  - **Reduces the size of all capacitors whose values are dictated by noise.**
- **Use multi-bit quantization**
  - **Reduces modulator order.**
  - **Increases b_1 (after performing voltage scaling), thereby reducing total capacitor area.**

3. 2-0 Cascade

Specifications

Parameter	Symbol	Value	Units
Bandwidth	f_B	1.25	MHz
Sampling Frequency	f_S	20	MHz
Signal-to-Noise Ratio	SNR	90	dB
Supply Voltage	VDD	5	V

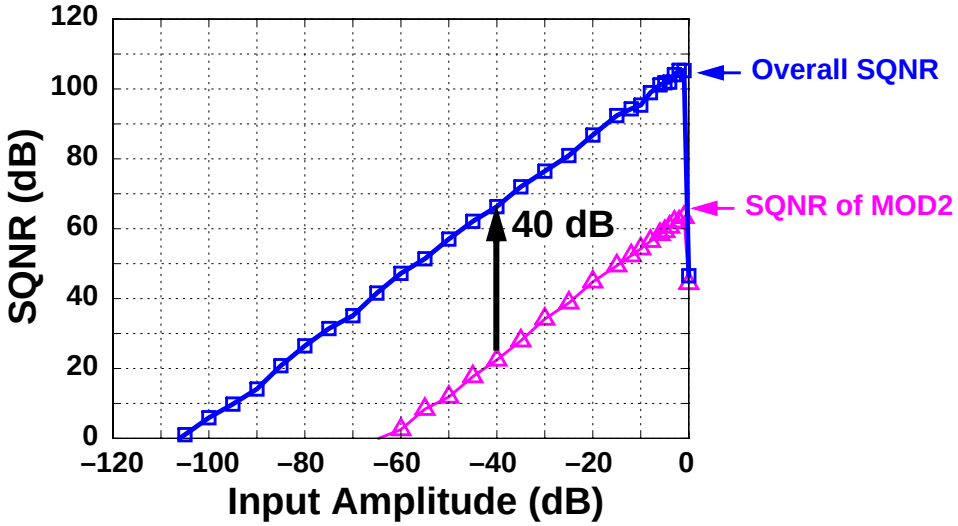
Simplified Block Diagram



Toolbox Evaluation

```
BW = 1.25e6; Fs = 20e6; OSR = Fs/(2*BW);
M = 32; nlev = M+1;
nb = 7; kpipe = 2^nb;
Ha = zpk([1 1],[0 0],1,1);
amp = [-120:5:-15 -12:2:-6 -5:0];
sqnr = zeros(2,length(amp));
N = 8192;
ftest = round(0.16/OSR*N);
u1 = M*sin(2*pi*ftest/N*[0:N-1]);
for i = 1:length(amp)
   [v1 junk1 junk2 y1] = simulateDSM(undbv(amp(i))*u1,Ha,nlev);
   v2 = ds_quantize(kpipe*(v1-y1),kpipe+1);
   v = v1 - filter([1 -2 1],1, v2/kpipe);
   spec1 = fft(v1.*hann(N))/(M*N/4);
   sqnr(1,i) = calculateSNR(spec1(1:ceil(N/2/OSR)),ftest);
   spec = fft(v.*ds_hann(N))/(M*N/4);
   sqnr(2,i) = calculateSNR(spec(1:ceil(N/2/OSR)),ftest);
end
plot(amp,sqnr(1,:),'m^','MarkerSize',10,'LineWidth',2);
hold on;
plot(amp,sqnr(1,:),'m--','LineWidth',3);
plot(amp,sqnr(2,:),'bs','MarkerSize',10,'LineWidth',2);
plot(amp,sqnr(2,:),'b-','LineWidth',3);
figureMagic([-120 0],10,2, [0 120],10,2);
```

Ideal SQNR Curve

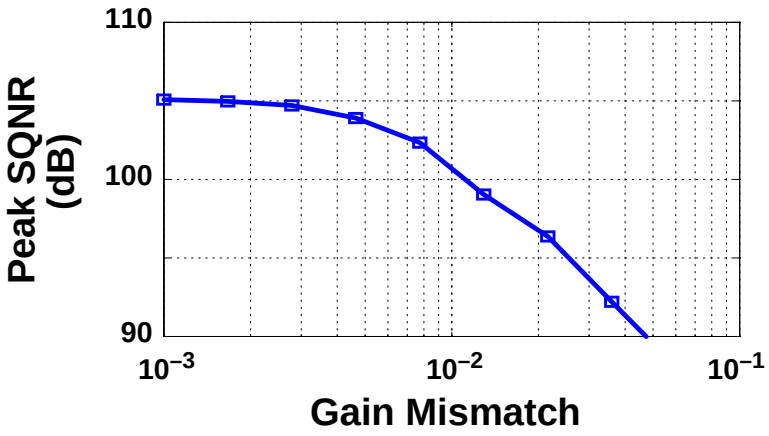


- **Simulated peak SQNR = 105 dB**

  Again, there is a lot of margin, so quantization noise should be small.

Gain Mismatch
(Capacitor Ratio Error)

```
v2 = ds_quantize(kpipe*(v1-y1)*(1+gain_mismatch),kpipe+1);
```

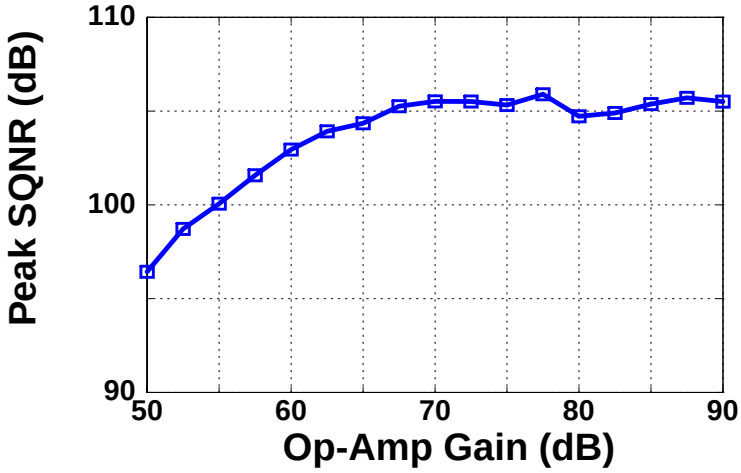


- **Need gain error < ~0.5%**

  Not a problem if moderately large capacitors are used.

NTF Zero Error
(Due to Finite Op-Amp Gain)

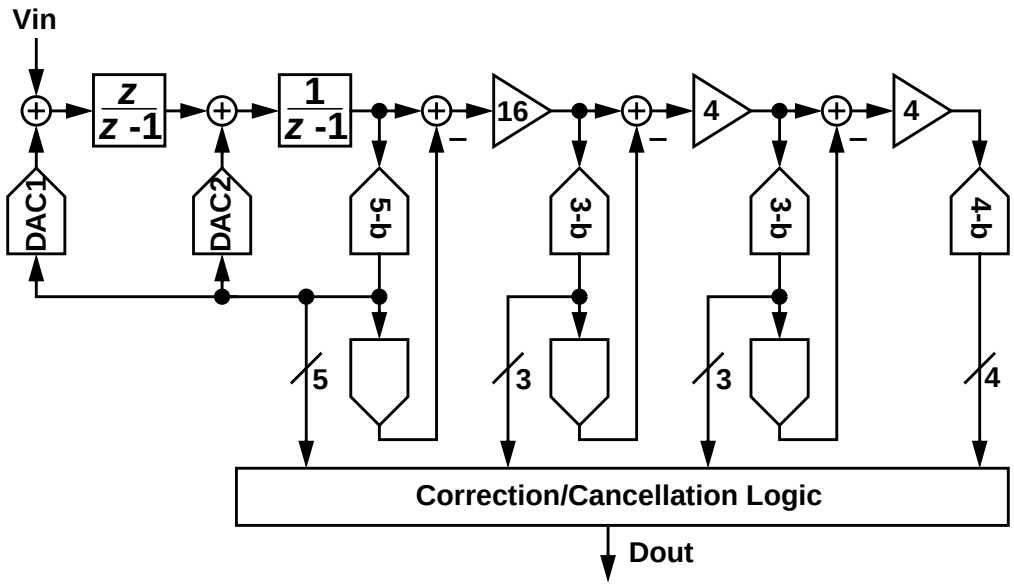
```
Ha = zpk([1 1]*(1-1/gain),[0 0],1,1);
```



- **Need op-amp gain > 65 dB**

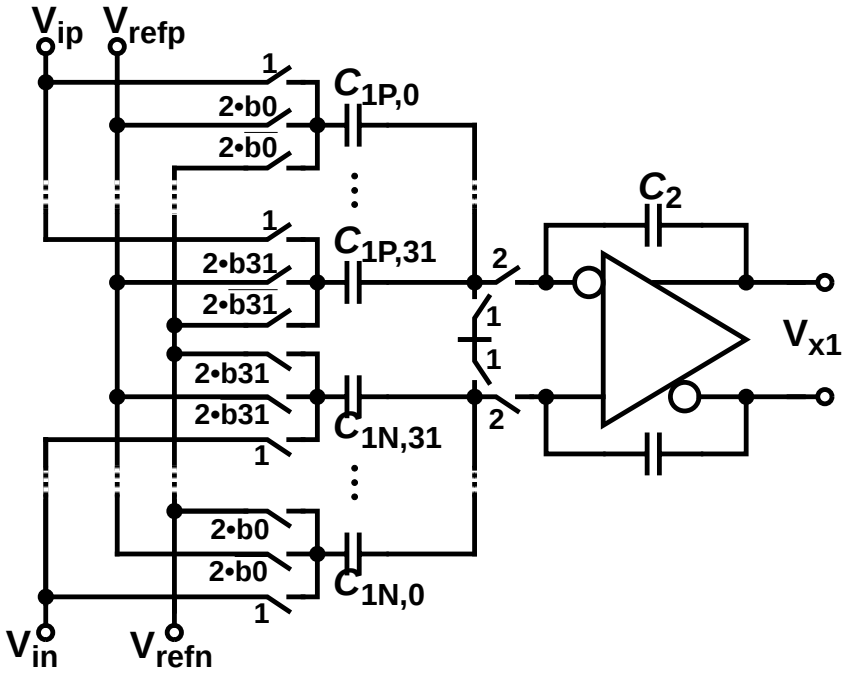
  Again, not an unreasonable requirement.

Block Diagram [Brooks 1997]

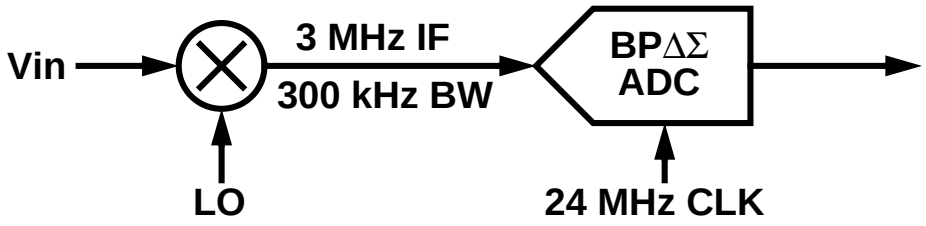


- **Has 1 bit of overlap at each stage**

An Integrator Stage



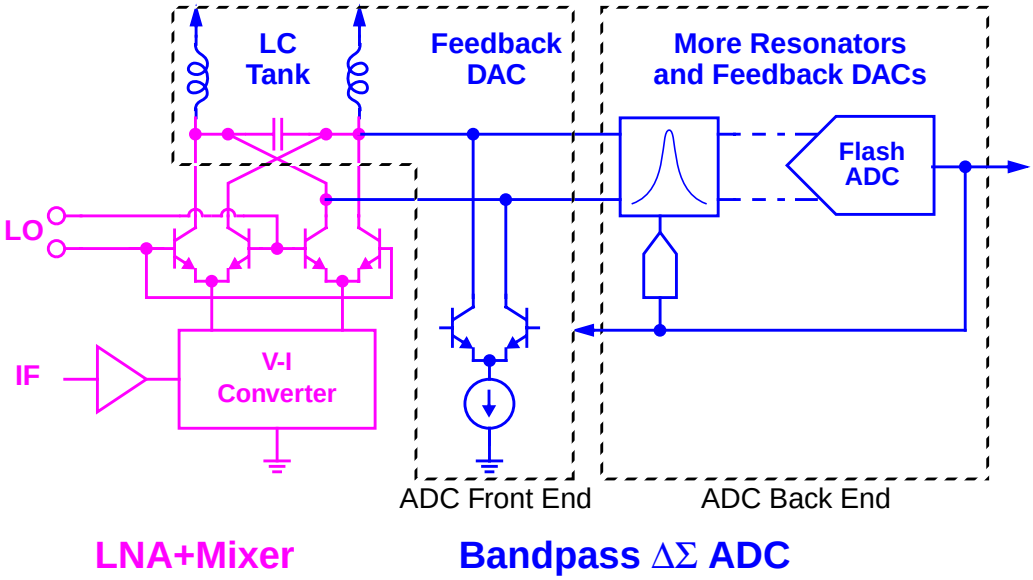
4. Bandpass Modulator



- **Want high dynamic range (~90 dB) with low power consumption (~50 mW)**
- **Desire a continuous-time architecture for its inherent anti-aliasing properties**
- **ΔΣ Toolbox indicates we should use a 6^{th}-order, 8-level modulator**

  Use a FB topology to get a clean STF.

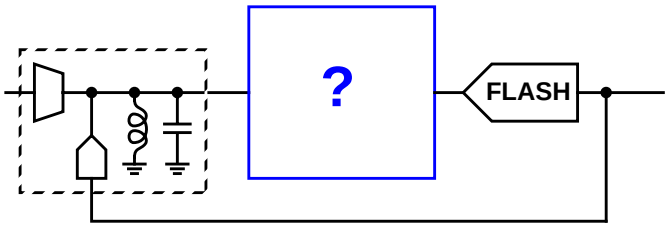
Simplified Architecture



Features of the Architecture

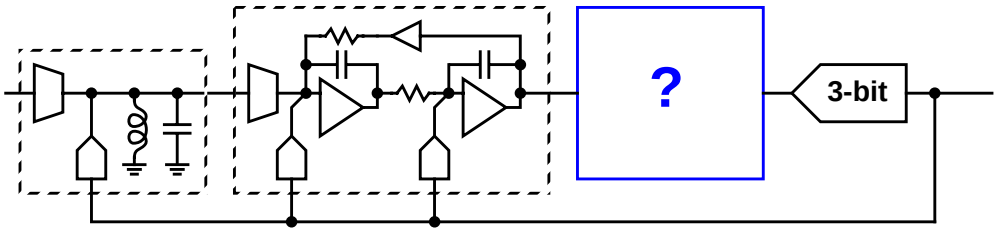
- **The mixer output current is processed by passive components which yield gain without adding noise or distortion, and without consuming power**
  - **More front-end gain makes back-end noise less important.**
- **The first feedback DAC cancels the bulk of the in-band portion of the mixer output, effectively passing only a residue to the ADC backend**
  - **Large signal-handling capability is not compromised.**
  - **Only the LNA, Mixer and ADC front end have to deal with the full dynamic range of the signal.**

Choices for the Second Resonator



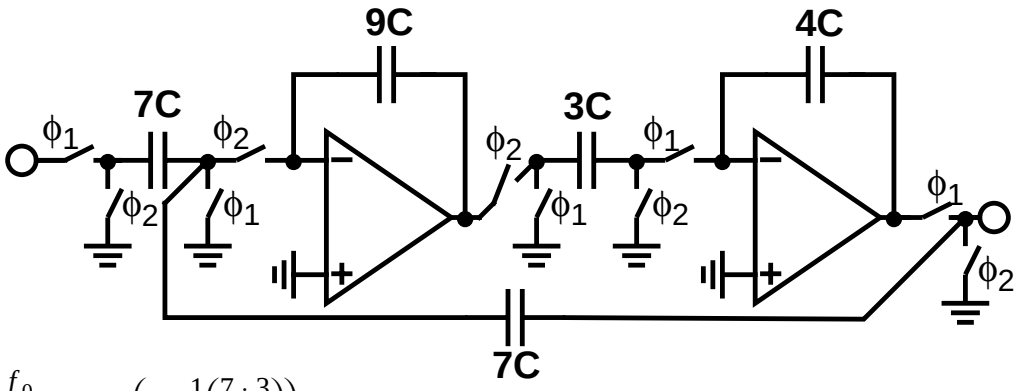
- **A second LC tank would require the least power, but would also need more pins**
- **Active-RC:2 mA for 50 nV/$\sqrt{\text{Hz}}$ i.r. noise**
  Switched-C:Estimate >10 mA for same i.r.n.
  g_m-C:Tough to get linearity and stability
  $\therefore$ Use Active-RC
- **Tuning implemented with 8-bit capacitor arrays**
  2:1 tuning range, regardless of process.

Choices for the Third Resonator



- **Active-RC:*Q* and drift are uncertain; might need a fourth resonator**
  Switched-C:*Q* is high (>100) and drift is low
  $\therefore$ Use Switched-C
- **Consumes 1 mA and has an i.r.n of 300 nV/$\sqrt{\text{Hz}}$.**

SC Resonator



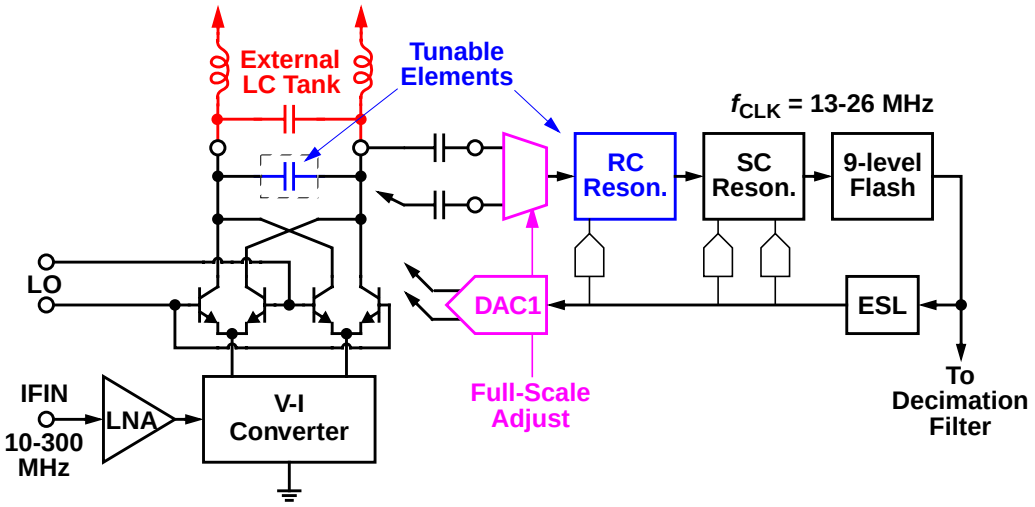
$$\frac{f_0}{f_s} = \text{acos}\left(1 - \frac{1}{2}\left(\frac{7 \cdot 3}{9 \cdot 4}\right)\right) = 0.1247$$

- **Center frequency is set by capacitor ratios**
  - **"LDI" structure guarantees pole on unit circle ($A = \infty$).**

AGC

- **For a –18 dBm input, the mixer output is 2 mA_{pp}, so DAC1 needs to sink 2 mA**
- **Power consumption can be reduced at low signal levels (the usual case) by reducing DAC1's full-scale**
  - **Reduces the FS of the ADC and thus gives the ADC more "gain."**
- **Lowering DAC1's full-scale also reduces the output current noise of the DAC**
  - **Includes mismatch-induced and dynamic errors as well as thermal noise.**
- **Placing a variable-gain element after the LC tank compensates for the reduced signal level and also saves current by minimizing the i.r.n. of the ADC's backend**

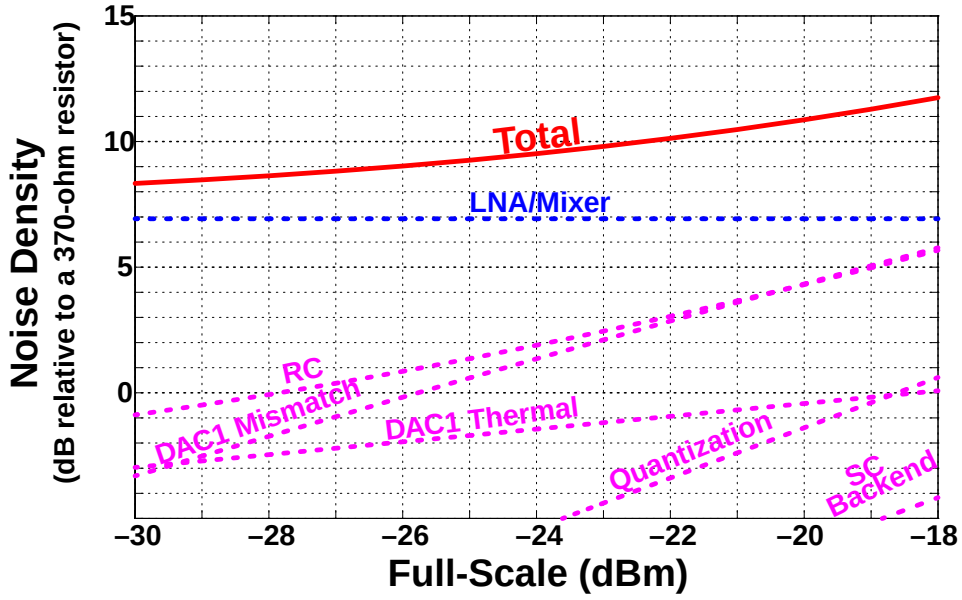
Full ADC



- **Achieves NF = 8 dB and IIP3 = 0 dBm with P = 50 mW**

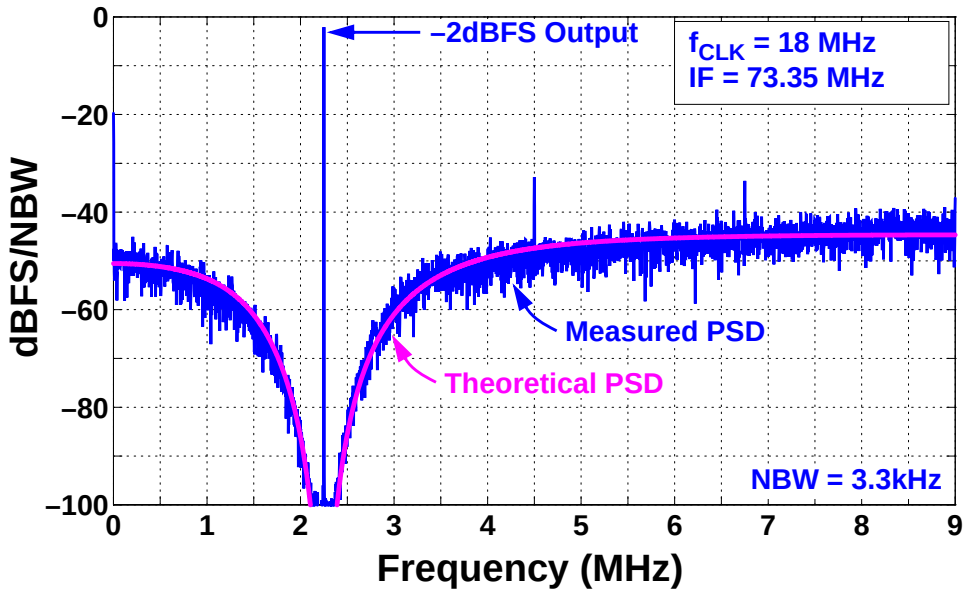
Noise vs. AGC

150 kHz BW



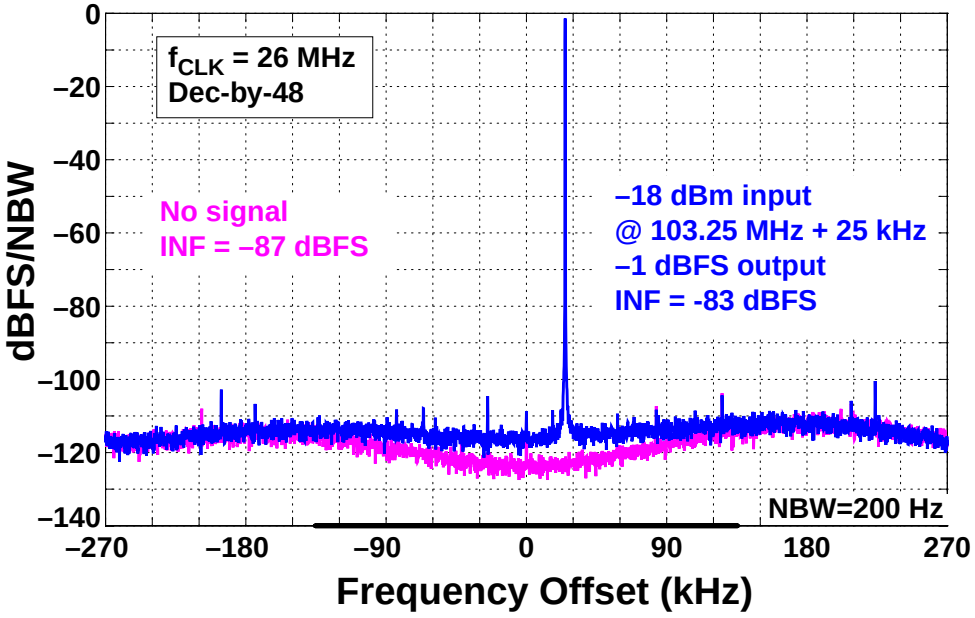
Spectrum of Undecimated Output

f_{CLK} = 18 MHz



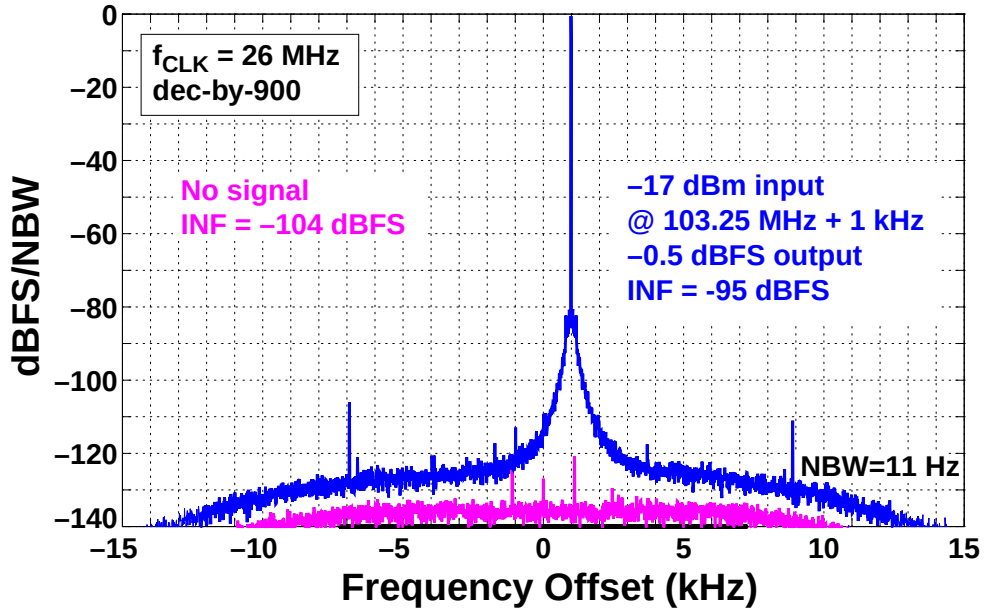
Spectrum of Decimated Output

BW = 270.833 kHz



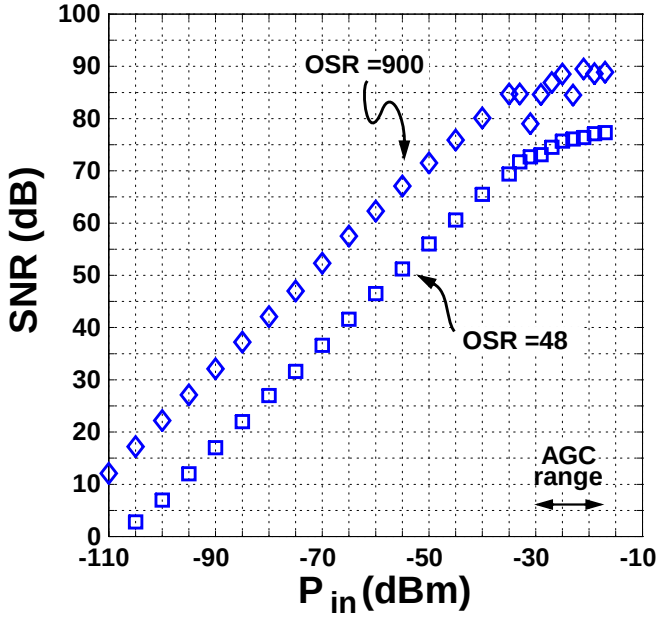
Spectrum of Decimated Output

BW = 15 kHz, 24-bit data



Measured SNR

f_{IF} = 273 MHz, f_{LO} = 269 MHz, f_{CLK} = 32 MHz



Summary

Design	OSR	DR (dB)	Lessons
MOD2	500	100	High OSR is helpful. ΔΣ can yield a very robust design.
MOD5	80	110	FF topology has lower cap. area than FB.
2-0 Cascade	8	90	Multi-bit quantization is needed to get high SNR at low OSR. Must be watchful of gain mismatch and NTF zero error in a cascaded system.
CT BP (LC)	48	85	An LC tank enables a power-efficient bandpass Mixer+ADC. The loop filter can use both continuous-time *and* discrete-time resonators.

- **Many design choices: ΔΣ/ΣΔ, single-loop/multi-loop, single-bit/multi-bit, lowpass/bandpass, discrete-time/ continuous-time, real/quadrature…**