History, Present State-of-Art and Future of Incremental ADCs

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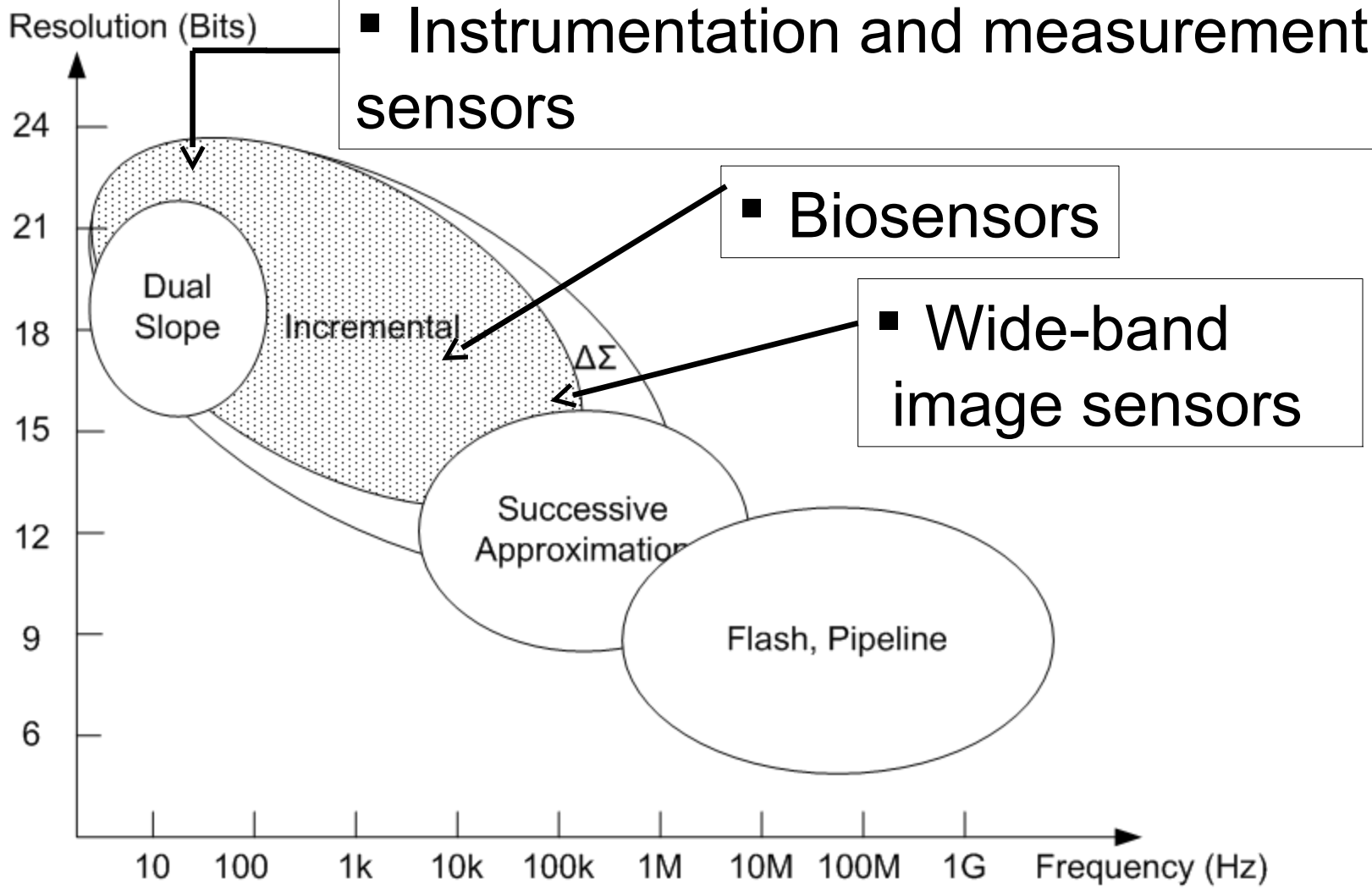
Sensor Applications

- Internet of Things (IoT) in homes and factories;
- Wearable devices (> 40 million sold);
- Product tags, RFID;
- Smart phones and watches;
- Imagers, MEMS systems, automobile sensors;
- Medical and environmental diagnostics.

The sensor and its interface are often powered by a small battery or only harvested energy, so low power dissipation is crucial!

Overview of ADC Performance



- Instrumentation and measurement sensors
- Biosensors
- Wide-band image sensors

ADC Options for I&M Applications

- **Dual-Slope ADC**

Very slow. Needs external components.

- **SAR ADC**

Limited resolution. Low INL is expensive (DAC trimming or digital calibration). Stringent anti-aliasing filter requirements.

- **Delta-Sigma ADC**

Offset and gain errors. Difficult to multiplex (settling time issues). Unlimited memory – tonal, may become unstable.

- **Incremental ADC**

Allows accurate offset and gain error correction.

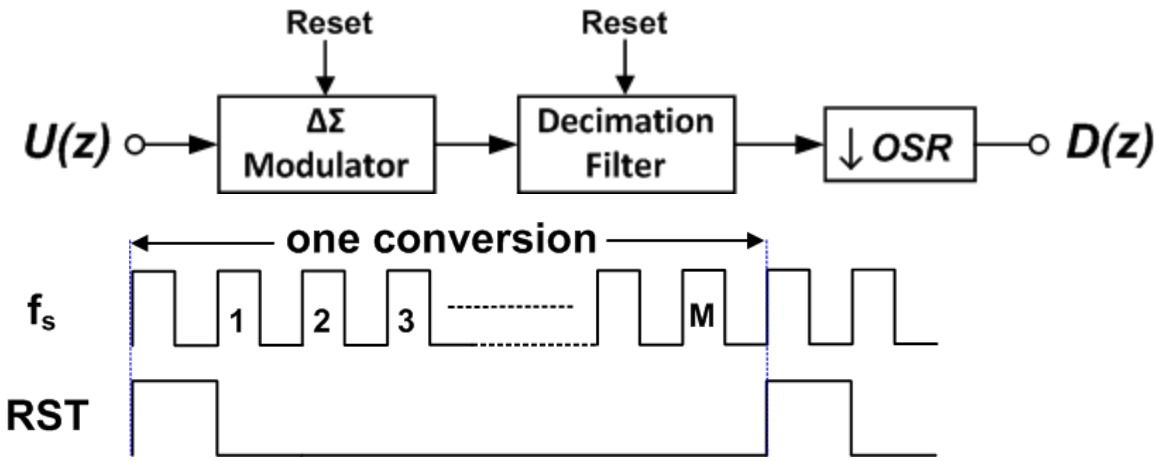
Limited memory –> not tonal.

Easy to multiplex. No need for external components, easiest signal conditioning. *Well suited for I&M applications!*

Incremental ADC vs. ΔΣ ADC

- The ΔΣ ADC has unlimited memory; it oversamples, and uses quantization error shaping.
- An incremental A/D converter (IADC) is a *periodically reset* ΔΣ ADC.
- The IADC acts as a ΔΣ ADC *between resets only*, to enhance its conversion accuracy.
- *The IADC performs as a memoryless (Nyquist-rate) ADC.*

Advantages of IADCs



- **Flexible trade-off** between OSR and power dissipation, bandwidth and sampling rate.
- **Low latency** from analog input to digital output.
- **Easy multiplexing** for multi-channel interface circuits.
- **Simple decimation filter**.
- **Multi-step operation** possible.

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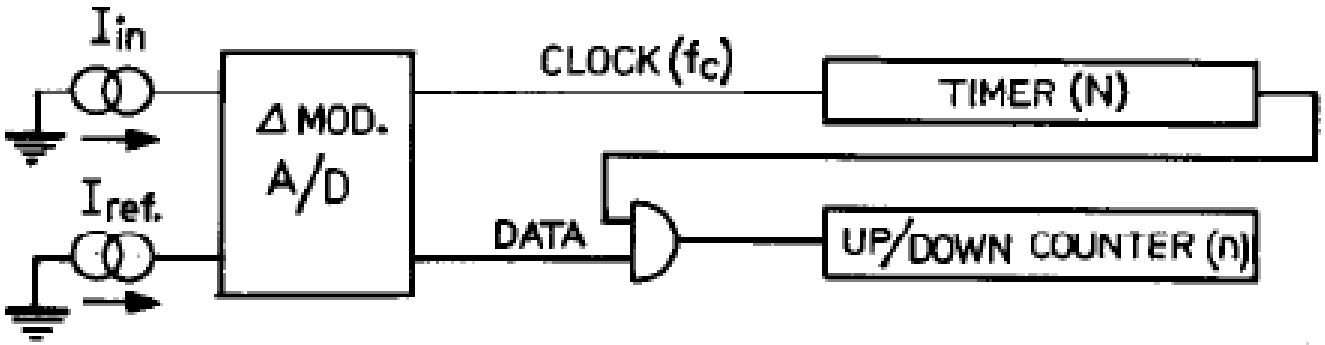
History – First IADC

- "A Sigma-Delta Modulator as an A/D Converter" J. van de Plassche, IEEE Transactions on Circuits and Systems, vol. CAS-25, no. 7, July 1978
- Current-mode circuit built from two bipolar analog ICs and added digital circuitry.



$$N = n_{up} + n_{down} \qquad n = n_{up} - n_{down} \qquad \frac{I_{in}}{I_{ref.}} = \frac{n}{N}$$

CONVERSION SPEED : $\frac{f_c}{N}$ RESOLUTION : N

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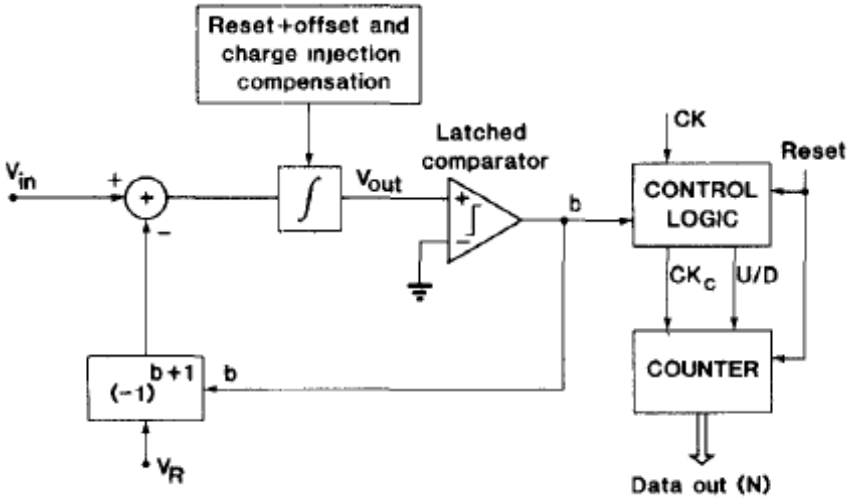
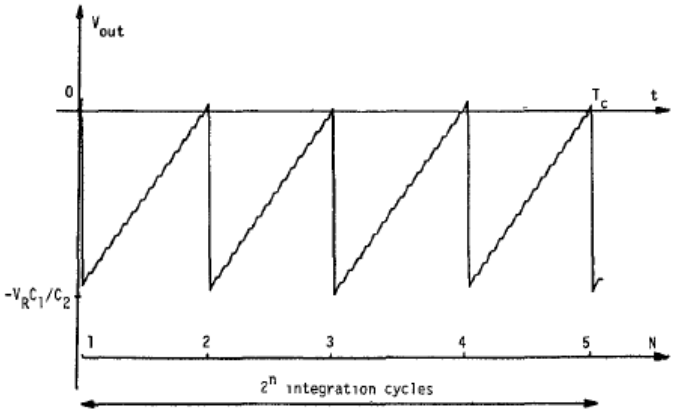
History – First DT CMOS IADC





Switched-capacitor implementation: Robert et al., JSSC 1987/4.

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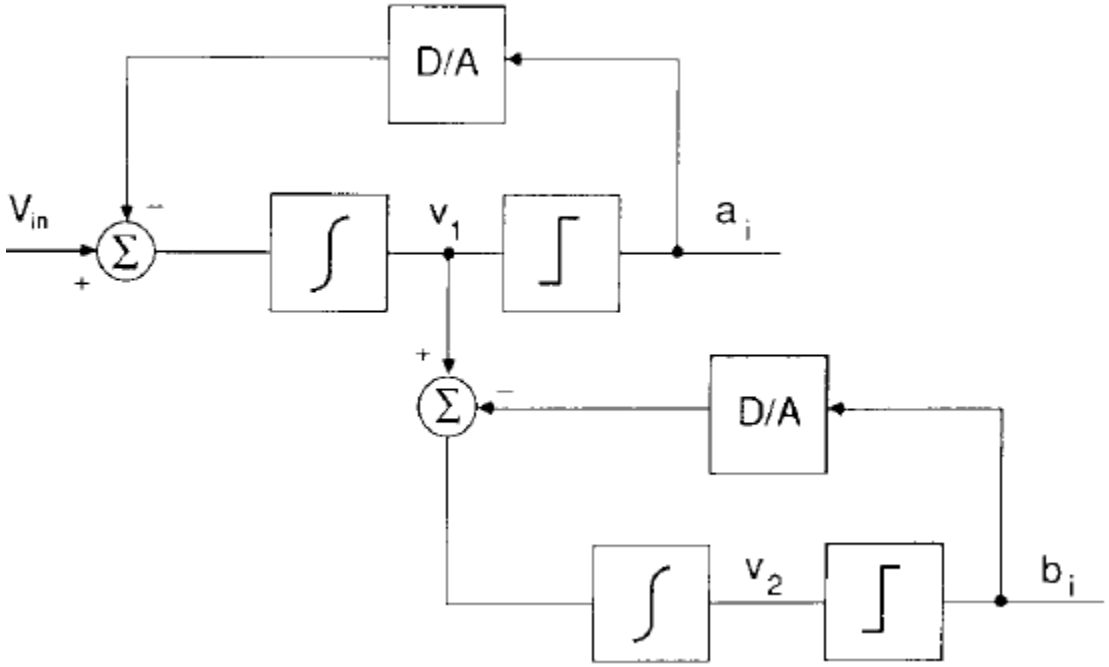
First MASH IADC

- A second-order (1+1) MASH SC incremental ADC [Robert et al.,JSSC 1988/3].



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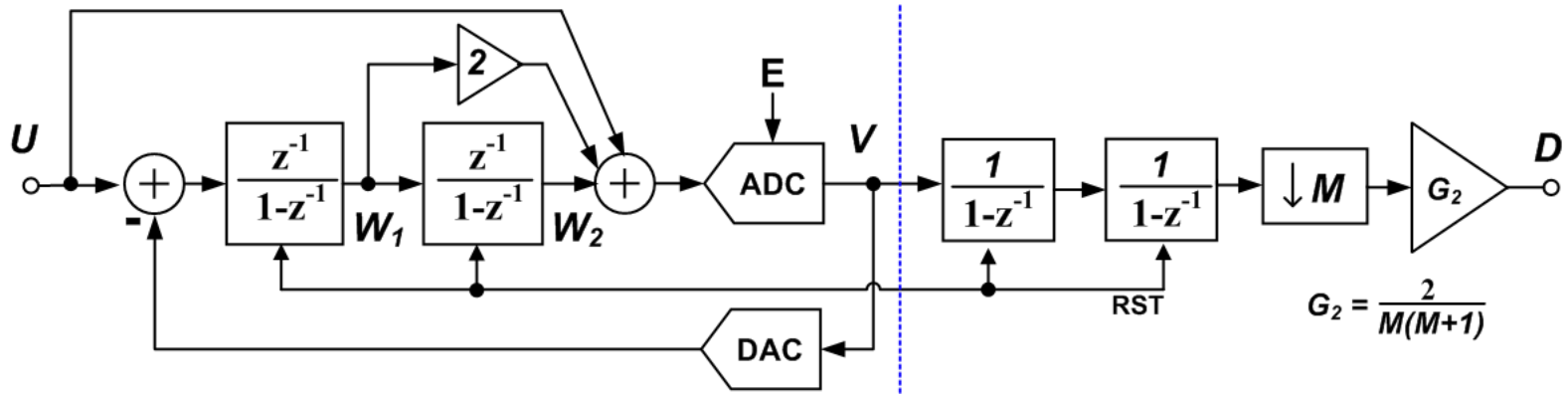
Higher-Order Single-Stage IADCs

2nd-order IADC

[Markus, TCAS-1 Apr., 2004]



*L*th-order IADCs:

- N-bit resolution IADCs require OSR= 2*N*/*L*.
- *L* opamps and peripheral circuitry needed.
- Worse stability and smaller non-overloaded range for large *L*.

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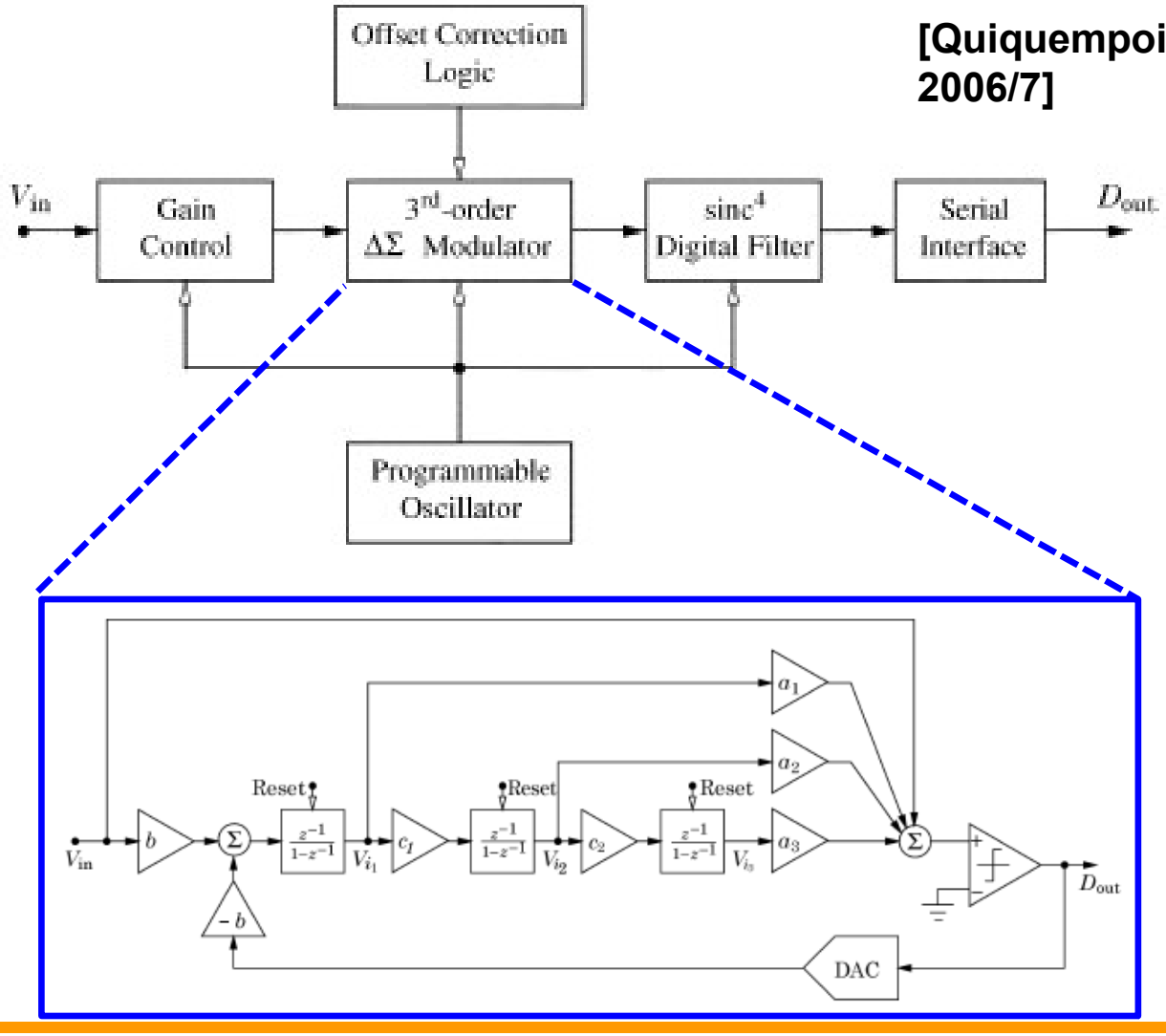
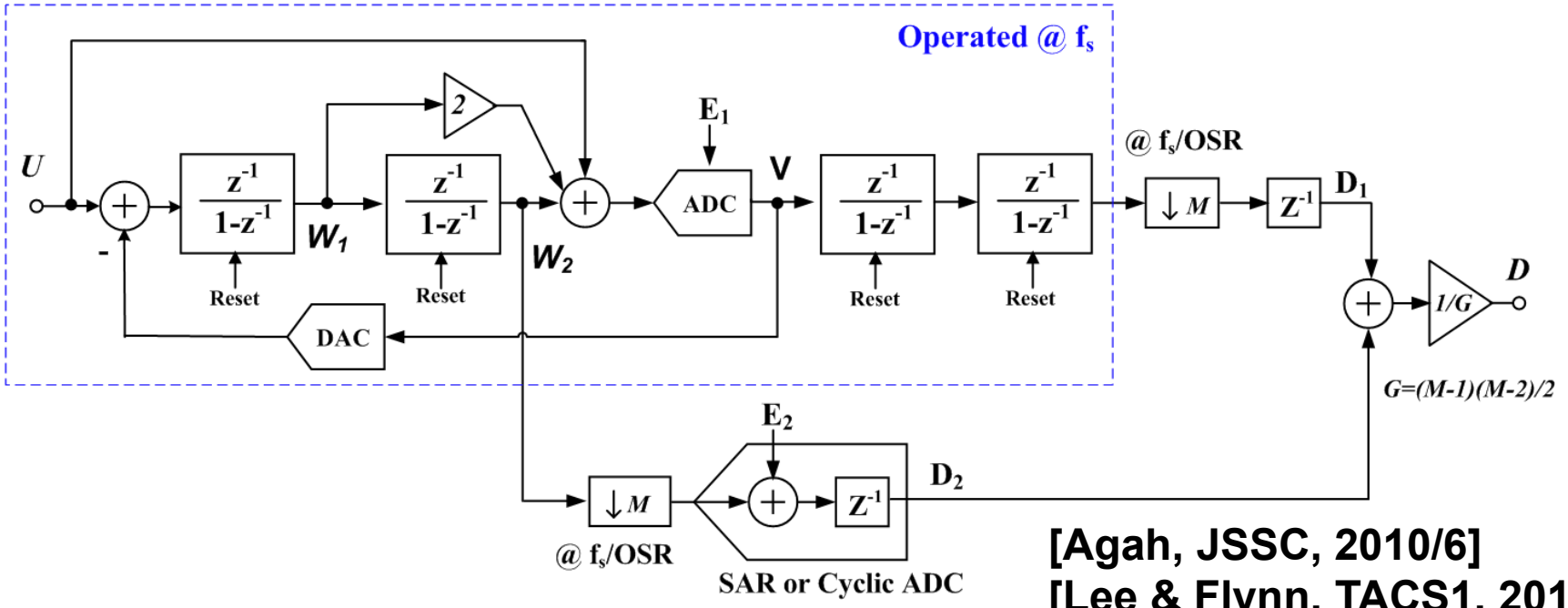
Prior Art: a 120 dB IADC

[Quiquempoix et al., JSSC 2006/7]



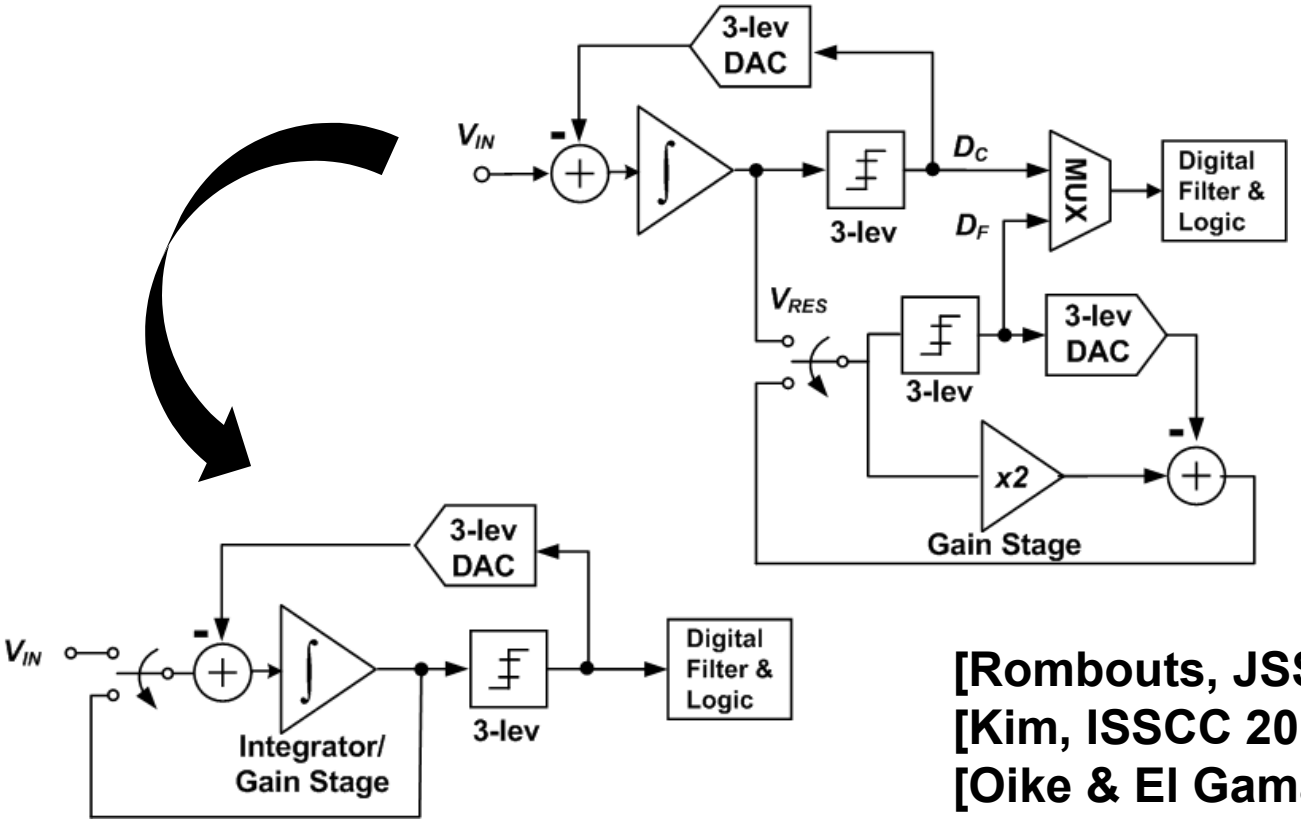
IADC with Extended Counting



[Agah, JSSC, 2010/6]
[Lee & Flynn, TACS1, 2011/6]

- Simpler decimation filter. No error cancelling logic needed.
- Low-power SAR or cyclic ADC can be the 2nd ADC.
- Complicated timing.
- Residue transfer needed: nonideal effects in SC circuitry limit accuracy.

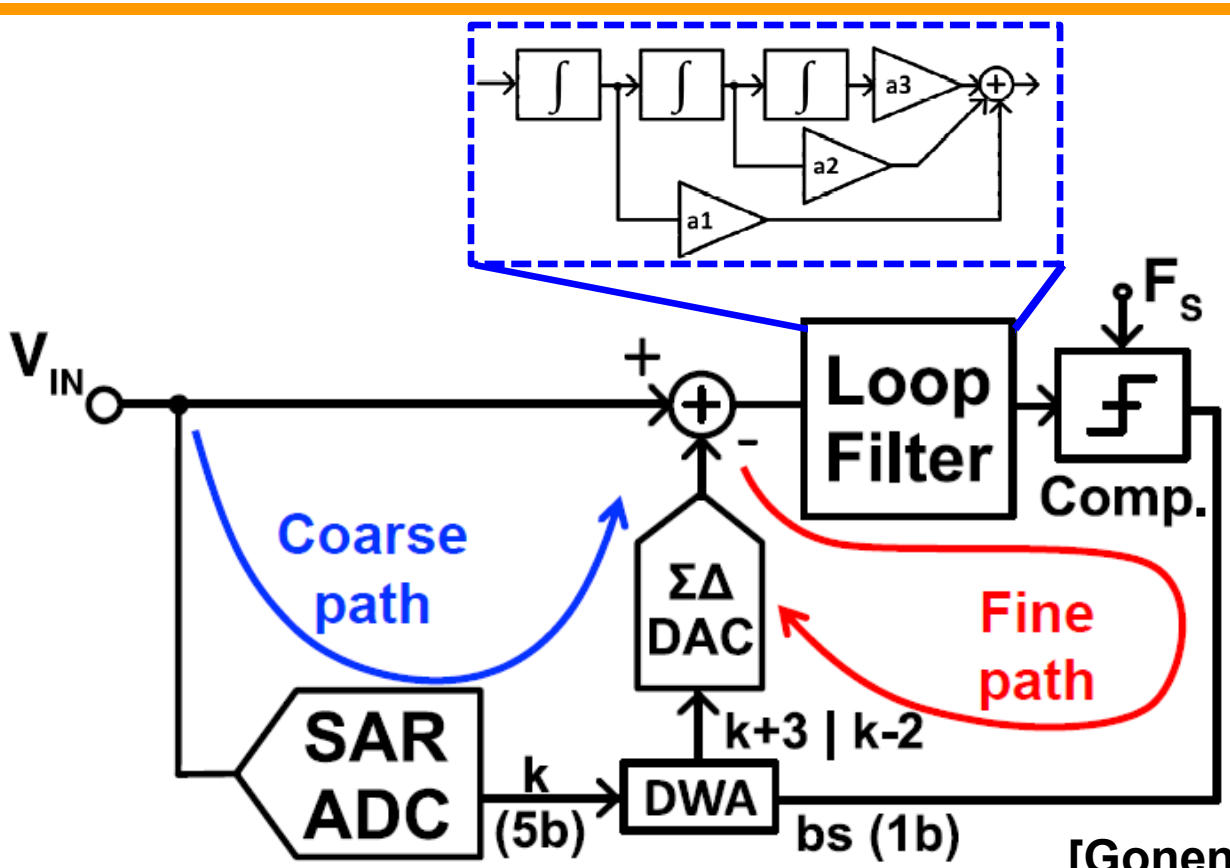
Extended Counting: Component Sharing



[Rombouts, JSSC 2001/2]
[Kim, ISSCC 2012]
[Oike & El Gamal, JSSC 2013/1]

- Two-step quantization: 1st-order IADC + Cyclic ADC;
- Complicated timing;
- Residue transfer needed, limiting the accuracy.

Dynamic Zoom ADC for 20 kHz BW



[Gonen, ISSCC 2016]

- Coarse: 5-bit SAR ADC.
- Fine: 3rd-order loop filter + 5-bit DAC.
- Peak SNDR=98 dB, 1.65mW, 20 kHz BW.

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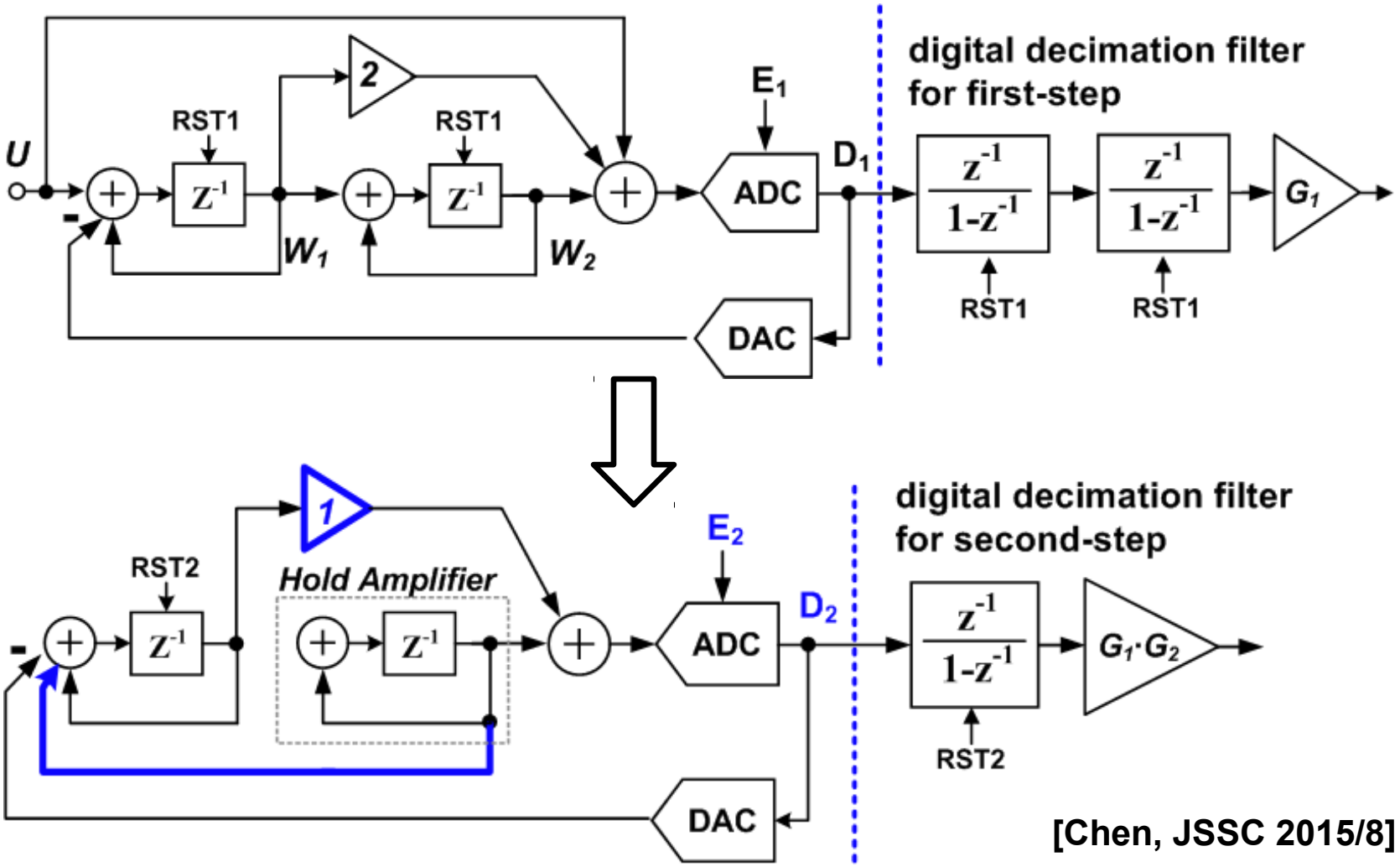
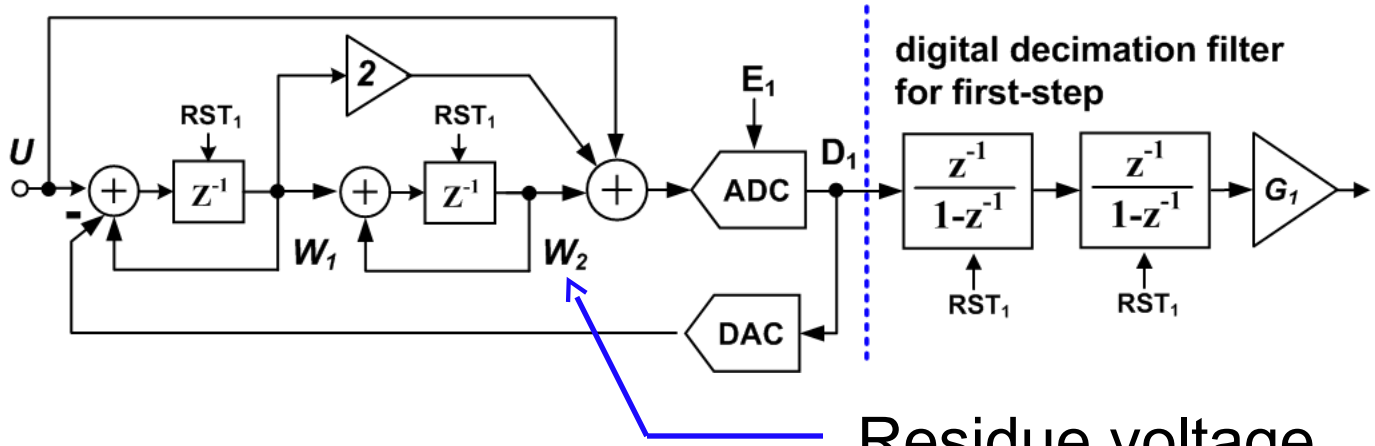
Two-Step IADC



[Chen, JSSC 2015/8]

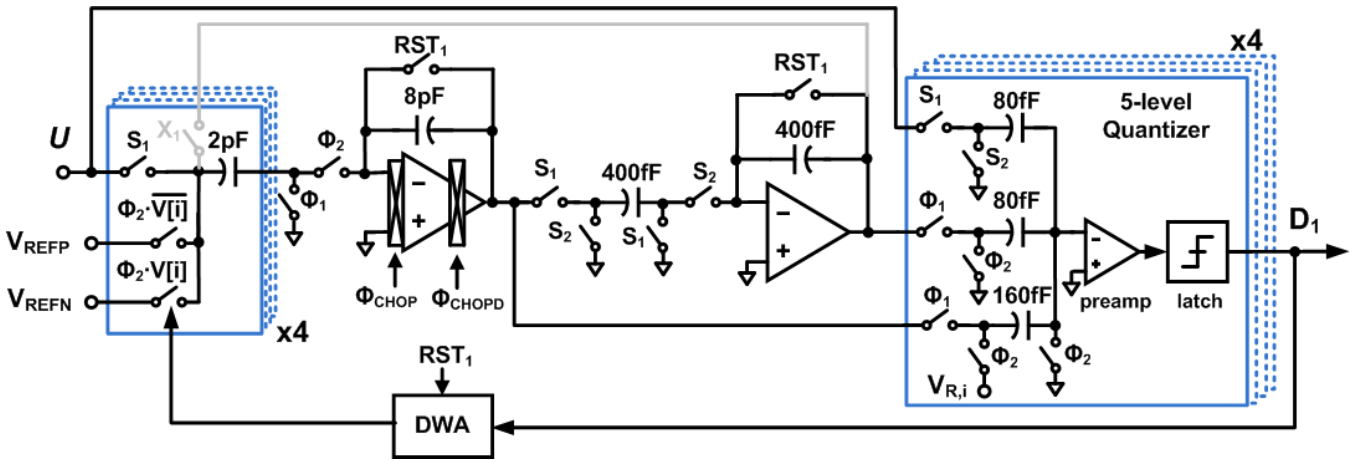
1st-Step Operation: 2nd-Order IADC

z-domain model; OSR=M1



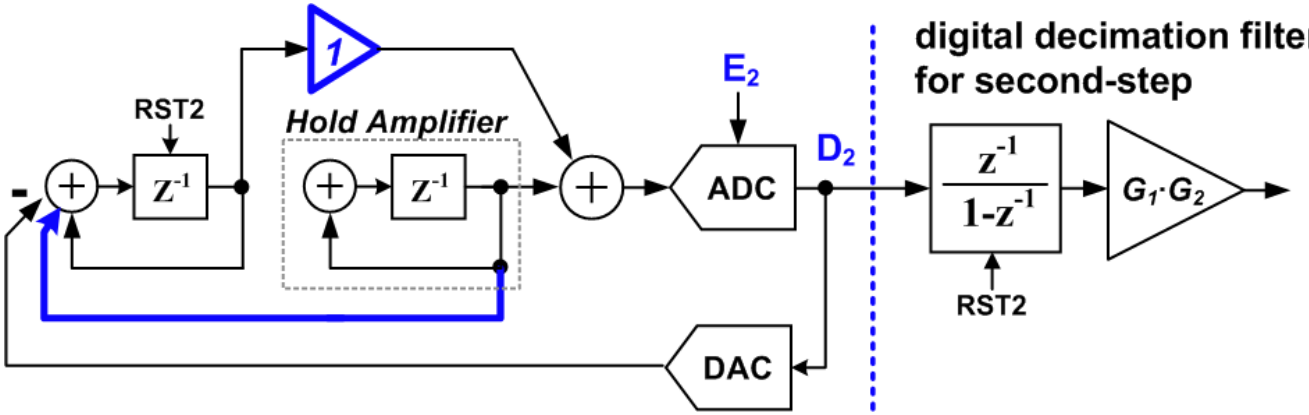
Residue voltage

SC circuitry

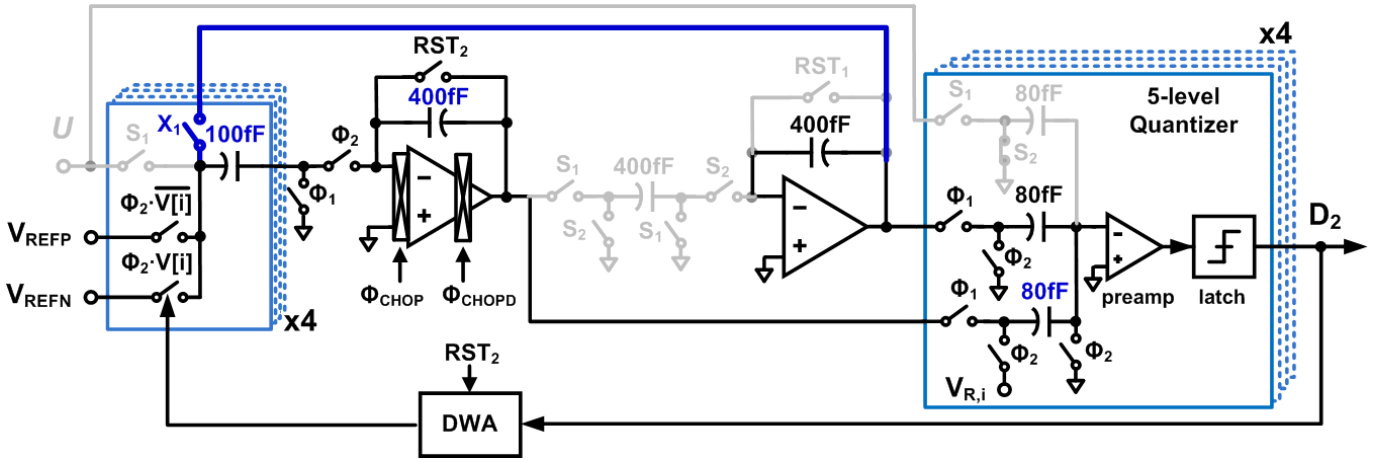


2nd-Step Operation: 1st-Order IADC

z-domain model; OSR=M2



SC circuitry



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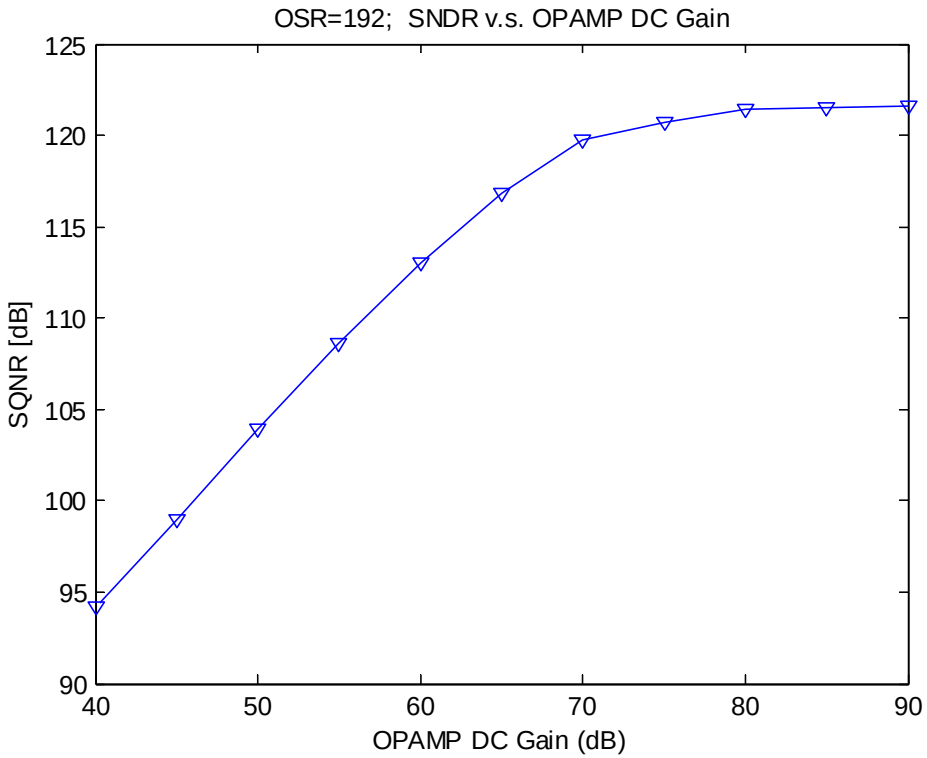
SNDR vs. Opamp DC Gain



- **Conventional MASH ΔΣ Modulators:**
  minimum opamp gain for SNDR > 100 dB: dc gain > **90dB;**
- **Two-step IADC:**
  SQNR falls below112dB only when the gain falls below **60dB!**

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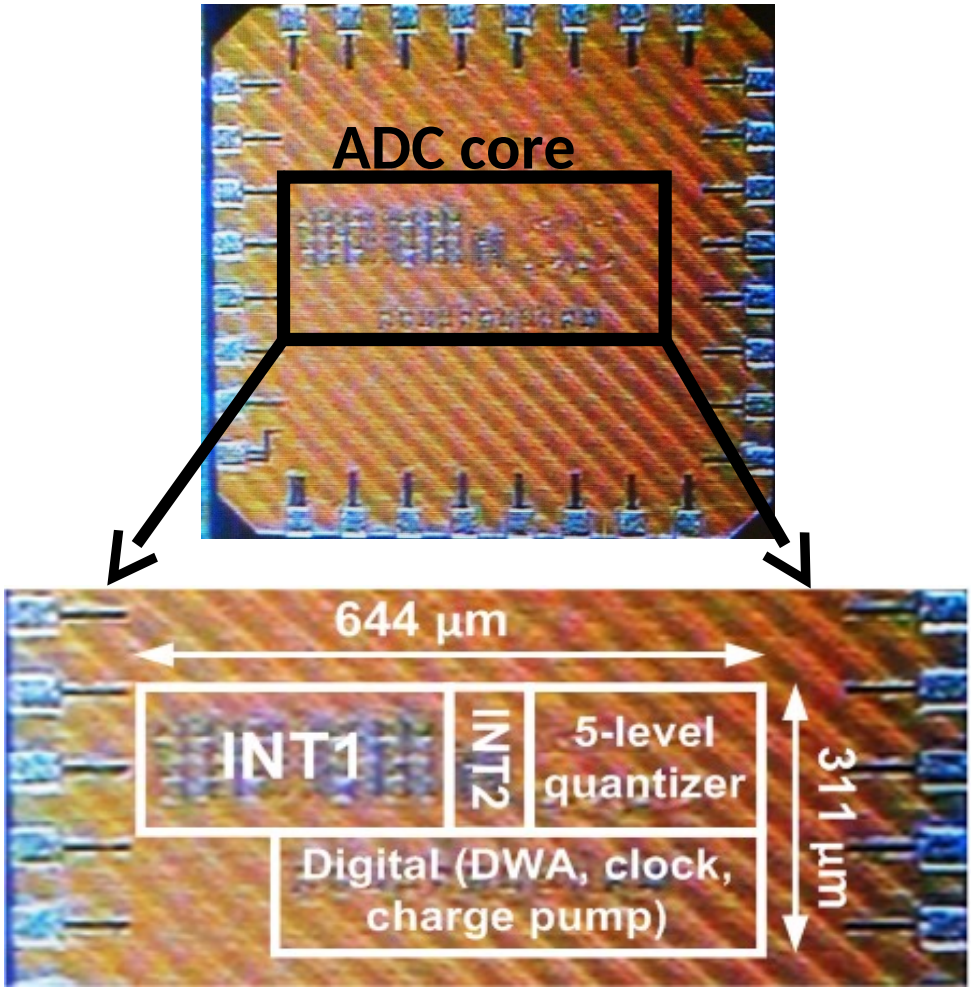
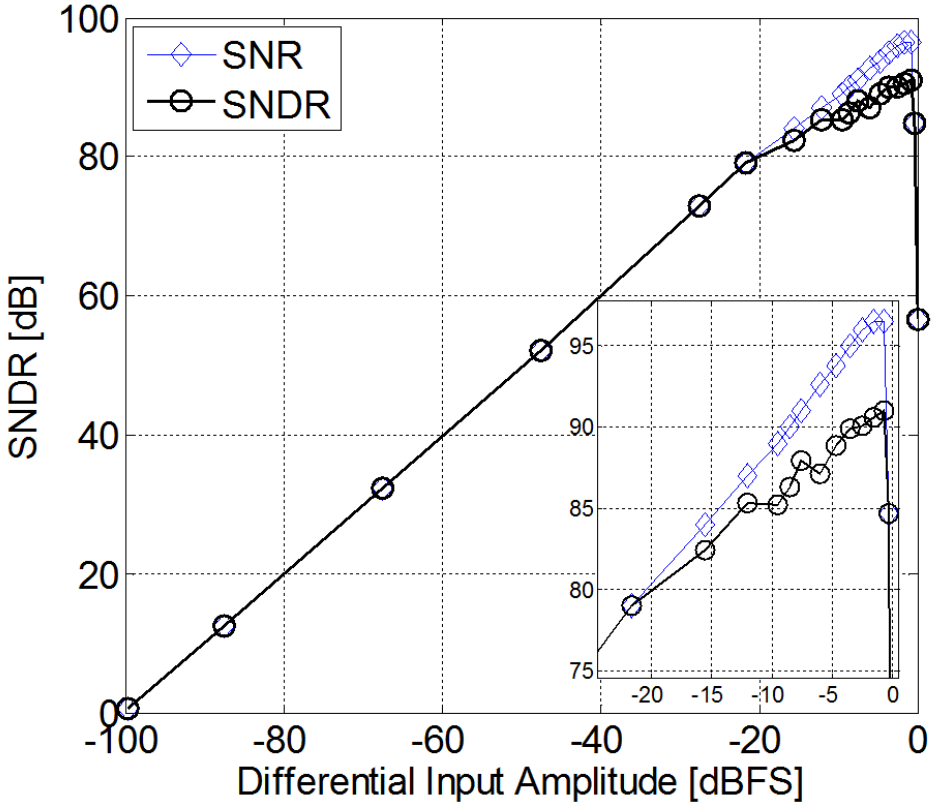
Die Photo


ADC core
644 µm
INT1
INT2
5-level quantizer
311 µm
Digital (DWA, clock, charge pump)

SNDR vs. Amplitude



- Differential full-scale reference = 2.4VPP (0dBFS)
- SNDRMAX = 90.8dB @ 2.2VPP (-0.76dBFS)
- Dynamic Range = 99.8dB relative to 2.2VPP (-0.76dBFS)

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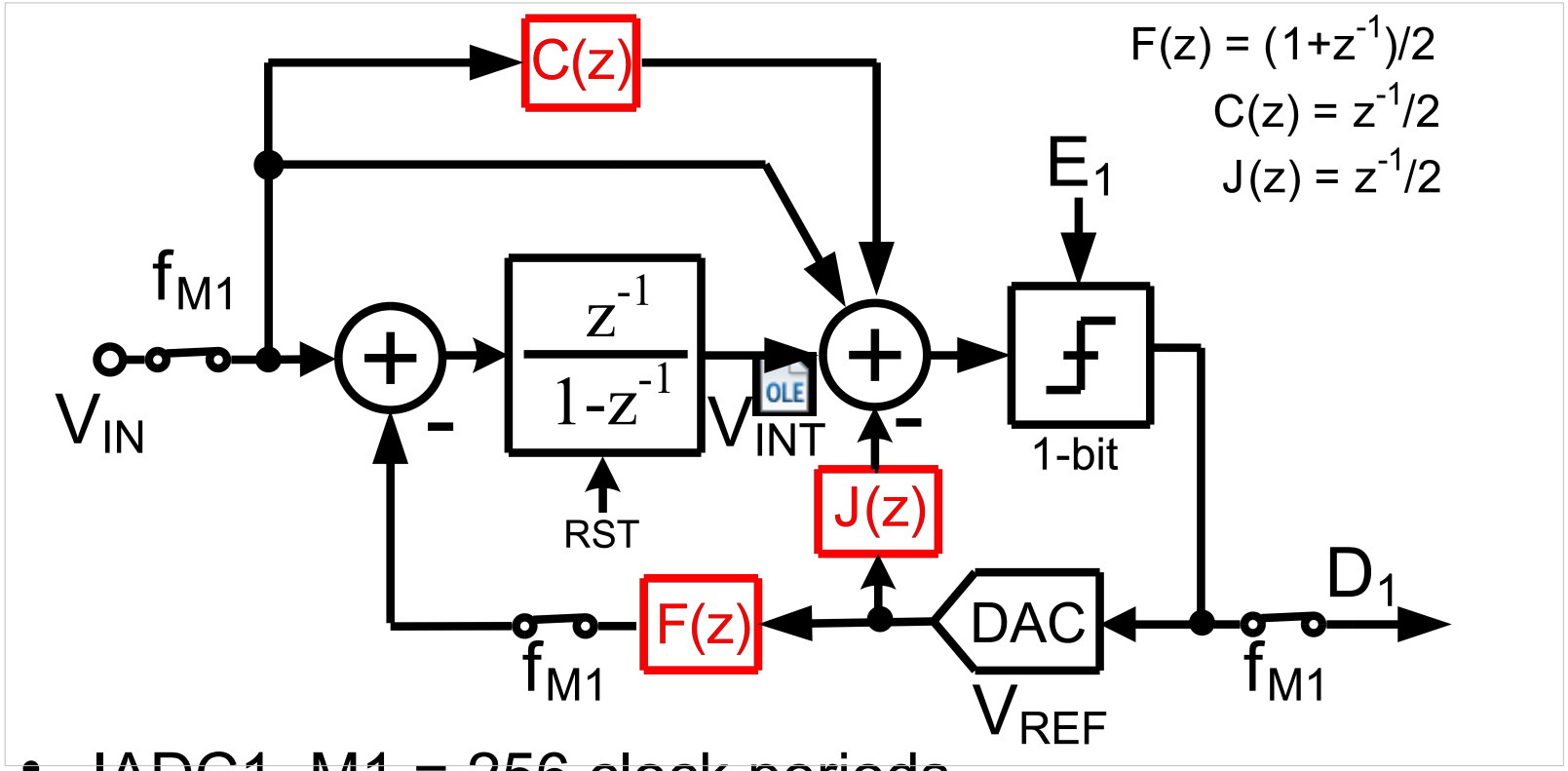
Performance Comparison

Parameters	This work JSSC 8/15'	Ha ESSCIRC 13'	Chae ISSCC 13'	Lee TCAS-I 6/10'	Agah JSSC 6/10'	Chen ISSCC 13'	Quiquempoix JSSC 7/06'
Architecture	IADC2 + IADC1	10b SAR + IADC1	6b SAR + IADC2	IADC2 + 10b cyclic	IADC2 + 11b SAR	single-loop IADC2	single-loop IADC3
Process	65 nm (2.5V MOS)	0.6 µm	0.16 µm	0.18 µm	0.18 µm	0.16 µm	0.6 µm
Area (mm2)	0.20	1.64	0.375	0.50	3.5	0.45	2.08
VDD (V)	1.2	3.3	1.8	2	1.8	1	3
Sampling frequency	96 kHz	5 MHz	50 kHz	115 MHz	45.2 MHz	750 kHz	30.72 kHz
OSR	192	256	400	5	45	80	512
Diff. input range	2.2 Vpp	2 Vpp	1.8 Vpp	3.6 Vpp	2 Vpp	0.7 Vpp	6 Vpp
Dynamic range (dB)	99.8	84.6	119.8	73	90.1	81.9	120
Peak SNDR (dB)	90.8	70.7	119.8	72	86.3	81.9	120
Bandwidth (Hz)	250 Hz	9.75 kHz	12.5 Hz	11.5 MHz	500 kHz	667 Hz	7.5 Hz
Power	10.7 µW	64 µW	6.3 µW	48 mW	38.1 mW	20 µW	300 µW
FoMW (pJ/Conv.-Step)*1	0.76	1.17	0.32	1.02	1.46	1.48	24.46
FoMS (dB)*2	173.5	166.4	182.8	156.8	161.3	157.1	164.0

*1Walden FoMW = Power/(2ENOB*2*BW)

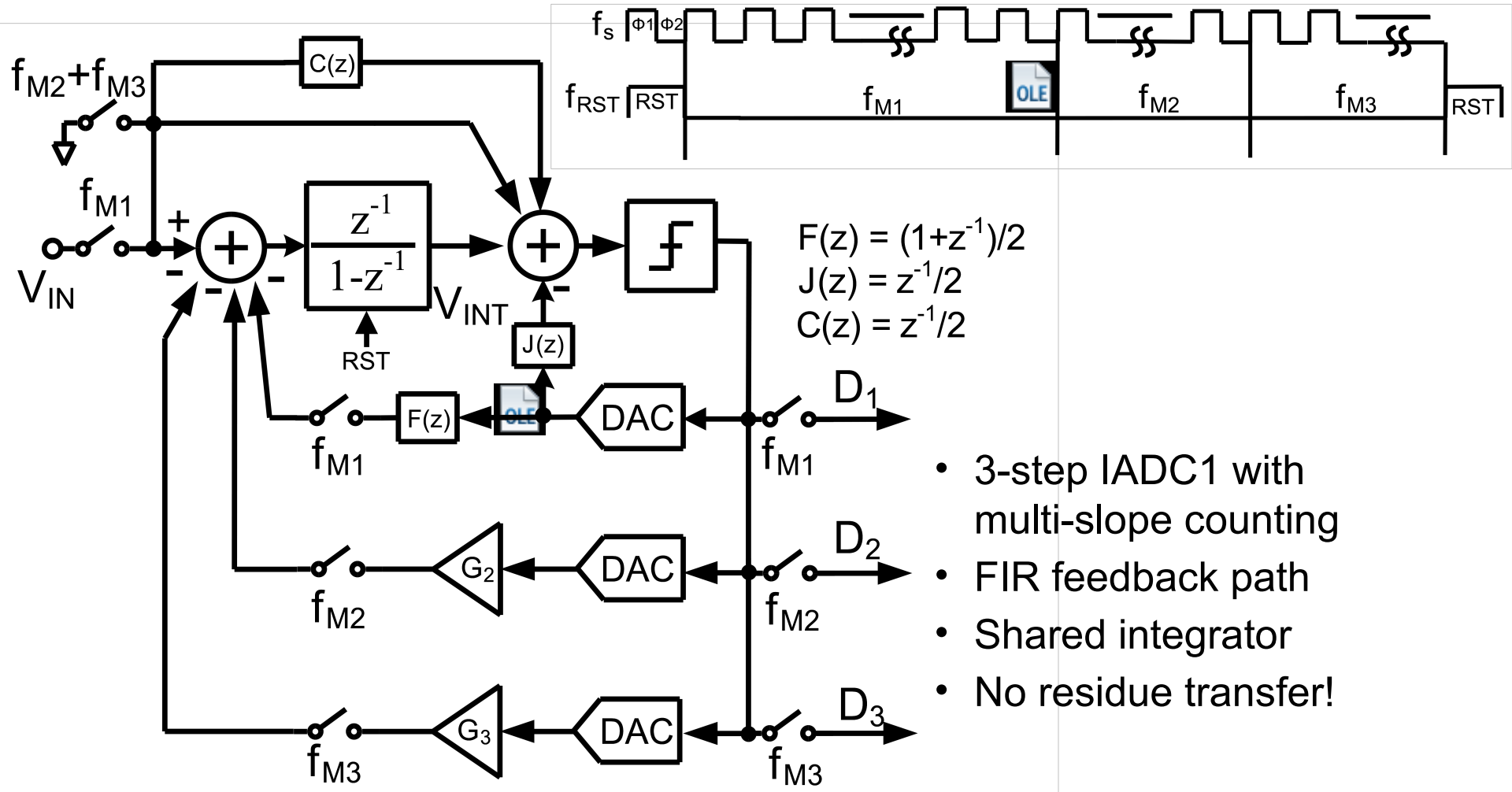
*2Schreier FoMS = DR + 10*log(BW/Power)

Error Cancellation Using Multi-Slope ADCs



- IADC1, M1 = 256 clock periods
- FIR feedback path F(z)
  - Reduces step size of VINT
- Quantization residue *E1* is stored as VINT

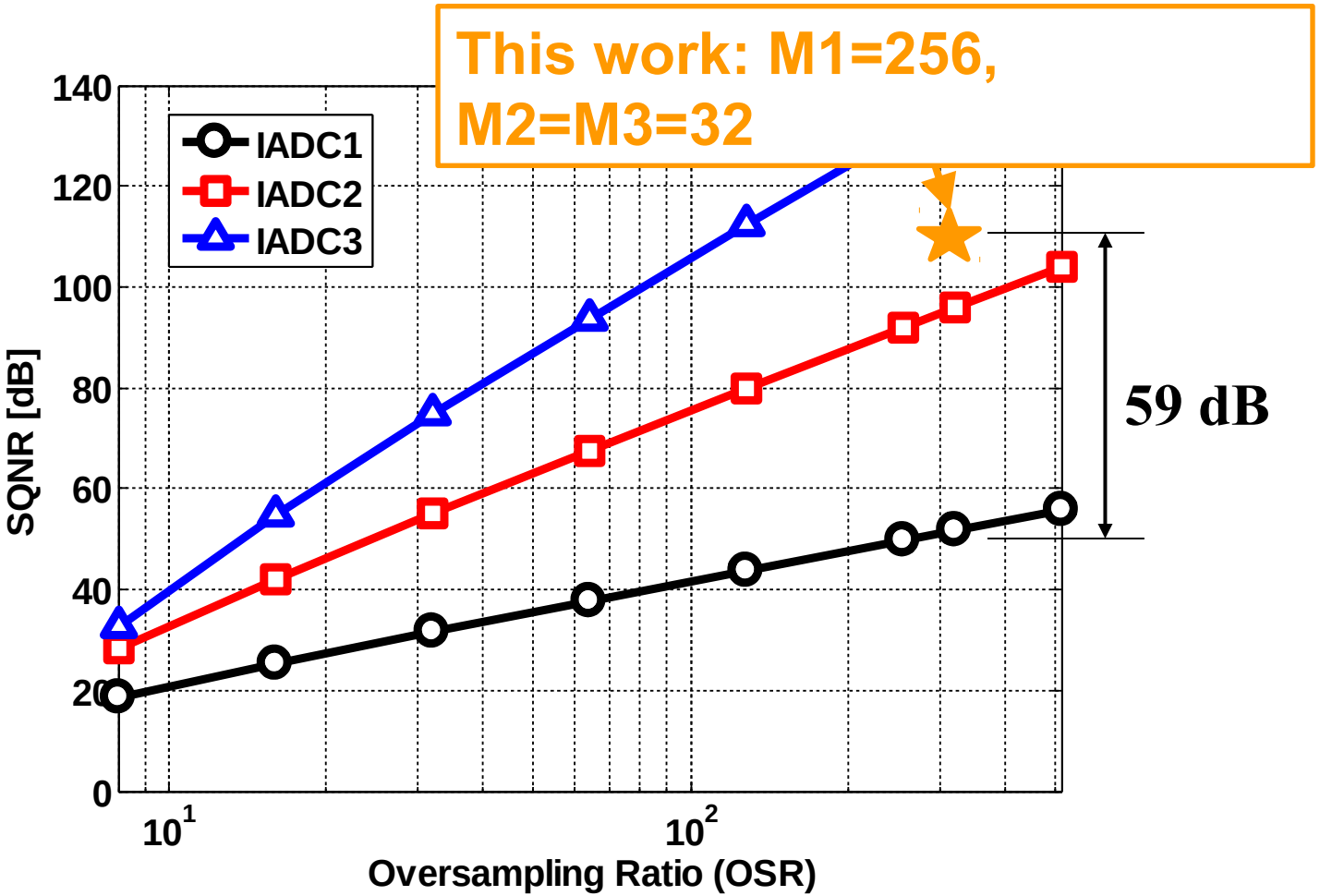
Overall Architecture



- 3-step IADC1 with multi-slope counting
- FIR feedback path
- Shared integrator
- No residue transfer!

[Zhang , VLSI Symp. Circuits, 2016]

SQNR Comparisons



- SQNR of proposed first-order loop with multi-slope counting.

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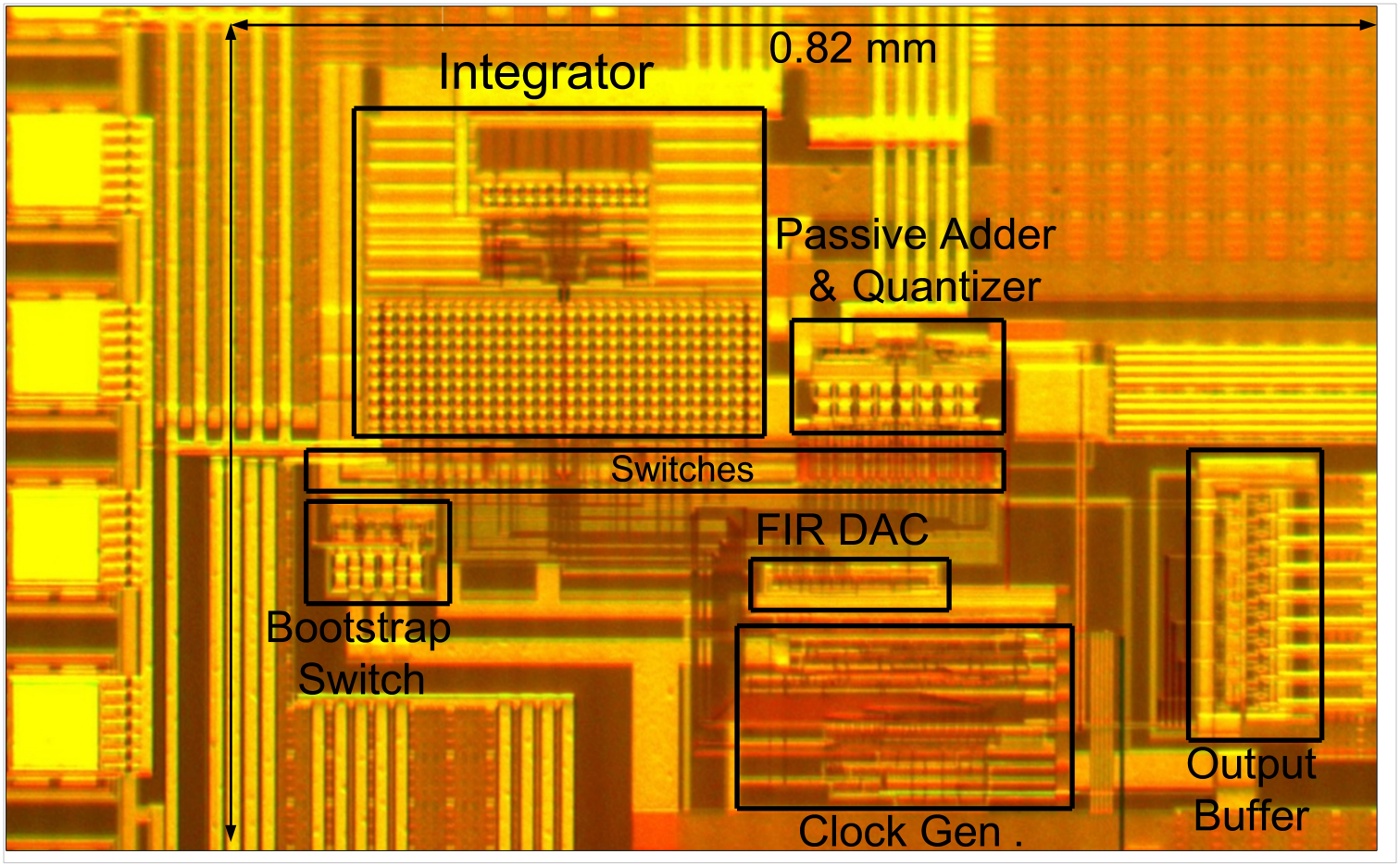
Die Photo

- Technology: 0.18 µm CMOS; Core area: 0.5 mm2



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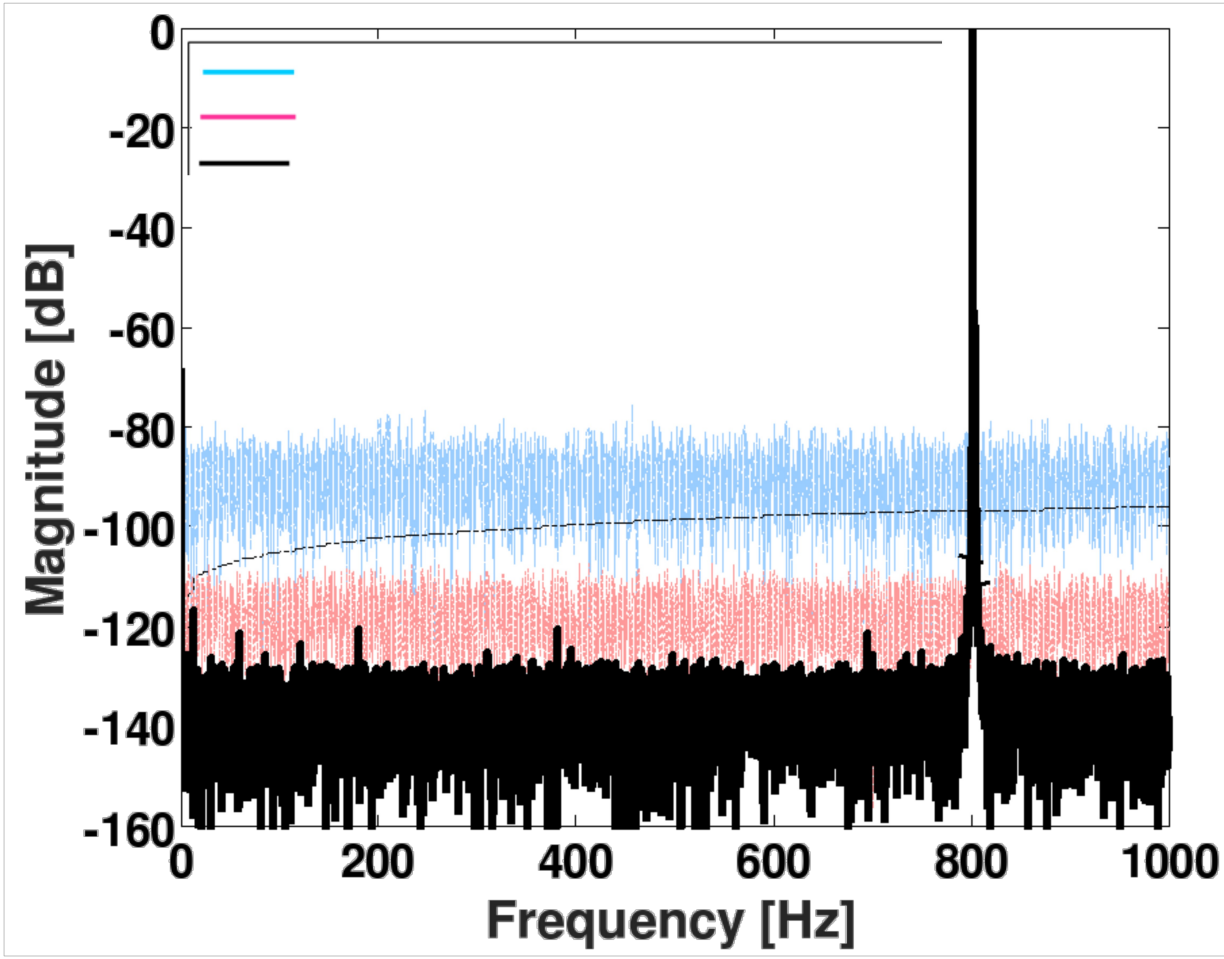
Measured Spectra (Cont'd)

- -0.5 dBFS, 800 Hz input



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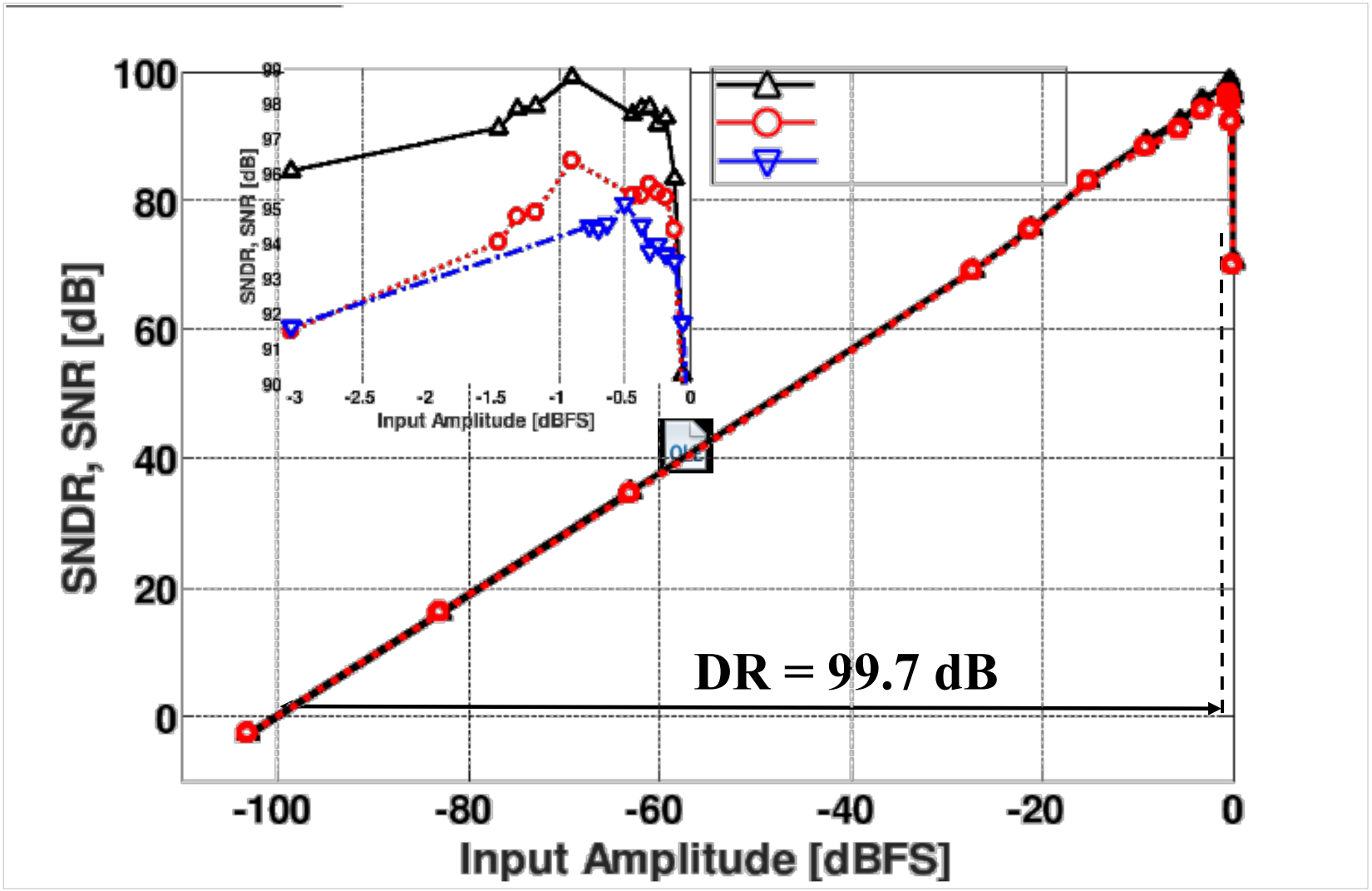
Dynamic Range



Performance Summary

Parameter	This Work	Chen JSSC 2015	Tao TCASI 2015	Goenen ISSCC 2016	Chen ISSCC 2013	Rombouts JSSC 2001	Agah JSSC 2010
Architecture	IADC1 + Multi-Slope	IADC2 +IADC1	CT IADC	Zoom ADC	Single IADC2	IADC1 + Cyclic	IADC2 + SAR
Technology	0.18 µm	65 nm	0.18 µm	0.16 µm	0.16µm	0.8 µm	0.18 µm
Area (mm^2)	0.5	0.2	0.337	0.16	0.45	1.3	3.5
V_{DD} (V)	1.5	1.2	1.2/1.8	1.8	1	1.2	1.8
Diff. input range	2 V_{PP}	2.2 V_{PP}	-	3.5 V_{PP}	0.7 V_{PP}	2.4 V_{PP}	2 V_{PP}
Sampling Freq.	642 kHz	192 kHz	320 kHz	11 MHz	750kHz	256 kHz	45.2MHz
Bandwidth	1 kHz	250 Hz	4 kHz	20 kHz	667 Hz	8 kHz	500 kHz
Power	34.6 µW	10.7 µW	34.8 µW	1.65 mW	20 µW	150 µW	38.1mW
Peak SNDR (dB)	96.5	90.8	07[illegible].9	98.3	81.9	80	86.3
Peak SNR (dB)	98.4	-	76.6	104.4	-	-	89.1
DR (dB)	99.7	99.8	85.5	107.5	81.9	82	90.1
FoM^1_W (pJ/conv)	0.32	0.76	0.61	0.32	1.48	1.15	1.46
FoM^2_S (dB)	174.3	173.5	166.1	178.3	157.1	159.3	161.3

1. $FoM_W = Power/(2^{(SNDR-1.76)/6.02} \times 2 \times BW)$. 2. $FoM_S = DR + 10 \times \log_{10}(BW / P)$

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Future Challenges

Increasing applications for robotics, IoT, wearable electronics and security will present new challenges:

- Reduced power dissipation for harvested-energy uses (may use continuous-time IADC, time-domain design, oscillator-based circuits).
- Wide-band operation for high-definition imagers.
- Design of single-chip SoCs containing sensors, AFE and wireless circuitry.
- IADCs for challenging environments (hot, cold, noisy, radiation) for automotive, aerospace, biomedical applications.

Conclusions

- Incremental ADCs offer energy-efficient A/D conversion for micro-power sensor interfaces;
- Their advantages include simple digital circuitry, reduced latency, ease of MUXing, robust stability, absence of idle tones, low-power multi-step operation;
- This talk described new techniques for multi-step IADCs with recycled active stages for further energy savings.