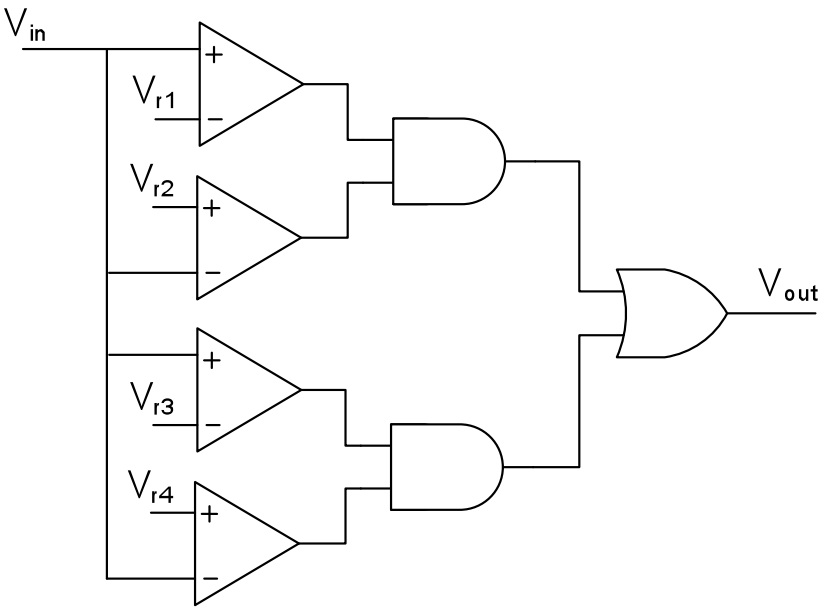
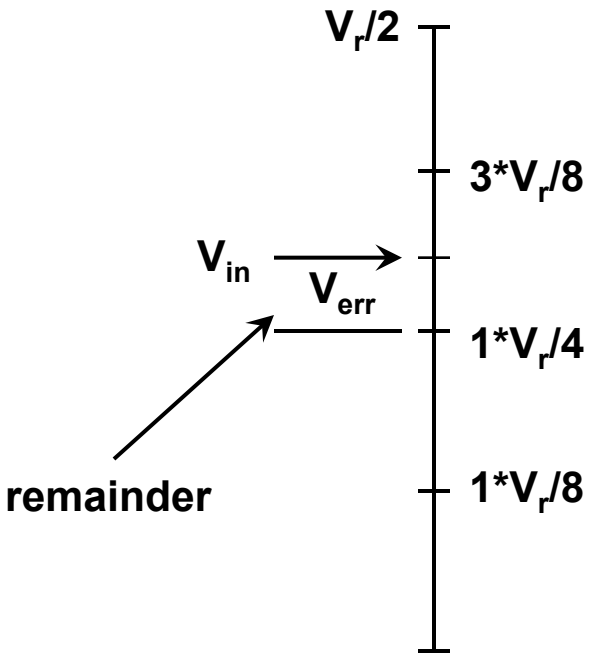
- Folding Block Implementation



- Folding ADC Output Logic Table

Code	2-bit MSB	V1	V2	V3	V4
15	11	1	0	0	0
14		1	1	0	0
13		1	1	1	0
12		1	1	1	1
11	10	0	1	1	1
10		0	0	1	1
9		0	0	0	1
8		0	0	0	0
7	01	1	0	0	0
6		1	1	0	0
5		1	1	1	0
4		1	1	1	1
3	00	0	1	1	1
2		0	0	1	1
1		0	0	0	1
0		0	0	0	0

Serial ADC Algorithms

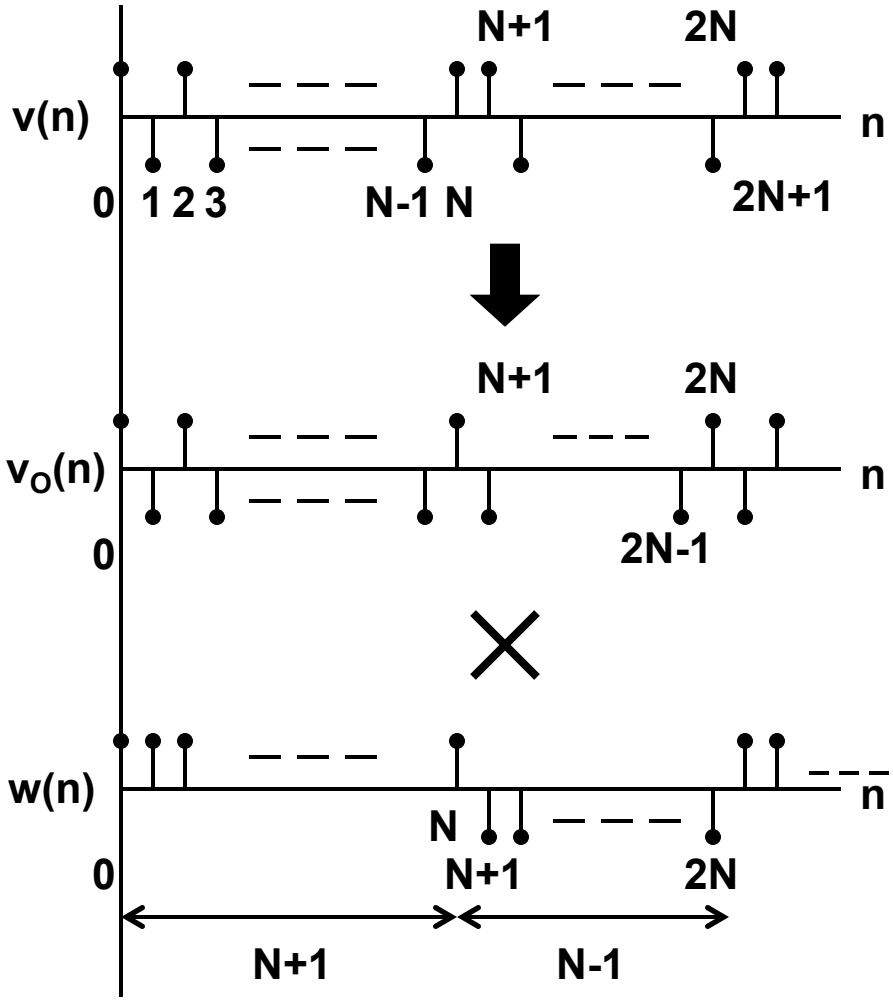


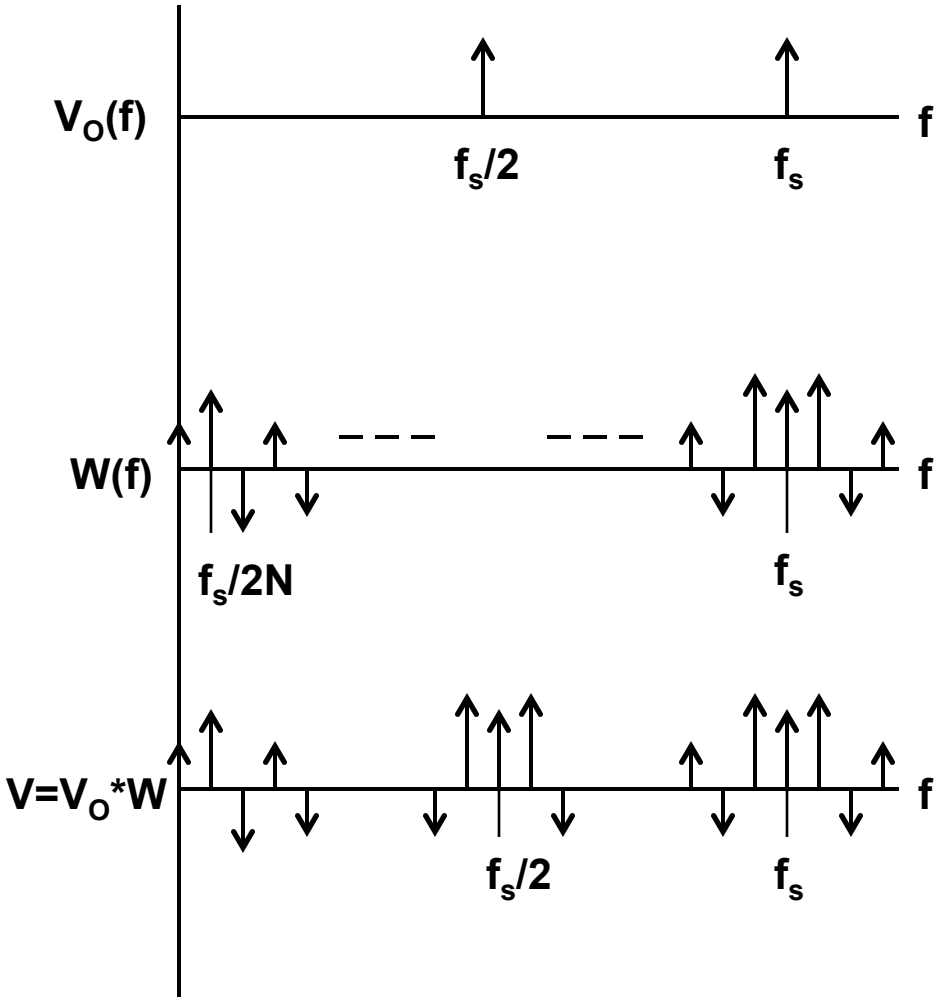
After finding $V_{in} > V_r/4$:

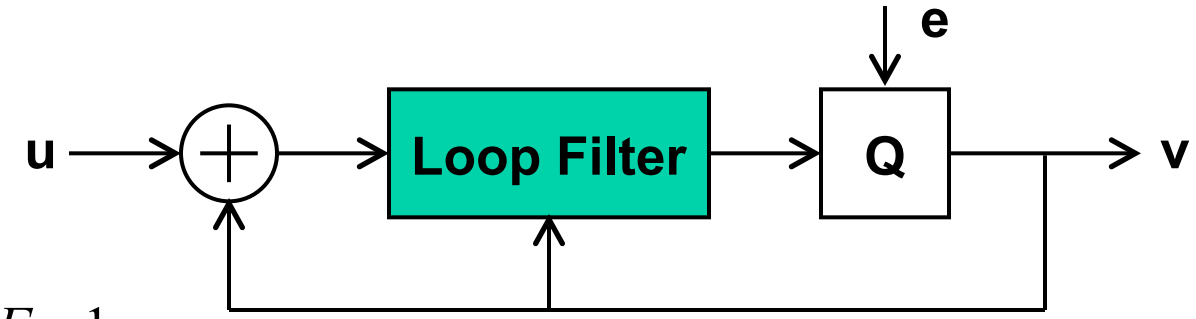
1. Divided reference algorithm:
   Vin >? $V_r/4 + V_r/8$?

2. Multiplied remainder algorithm:
   $2V_{err} = 2(V_{in}-V_r/4)$ >? $V_r/4$
   Same answer ! (“No”)

Inband Tone Generation







$$STF = 1$$

$$Y = U + [H - 1] \cdot E$$

$$y(n) = u(n) + [h(n) - \delta(n)] * e(n)$$

But $h(0) = 1$, since delay-free loops are not physical, so

$$y(n) = u(n) + \sum_{i=1}^{\infty} h(i) \cdot e(n - i)$$

$|y(n)|_{\max} \le M$ guarantees stability,

Initially $|e(n - i)| \le 1$,

Note that $h(0) = 1 \rightarrow H(z)\big|_{z \to \infty} = 1.$