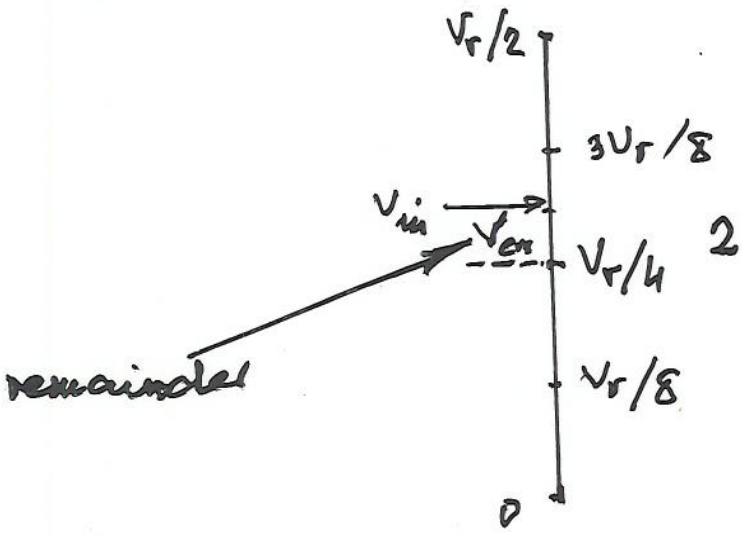
Serial ADC Algorithms

After finding $V_{in} > V_r/4$:



1. Divided reference algorithm:

$V_{in} \overset{?}{\geq} V_r/4 + V_r/8$?

↓

0

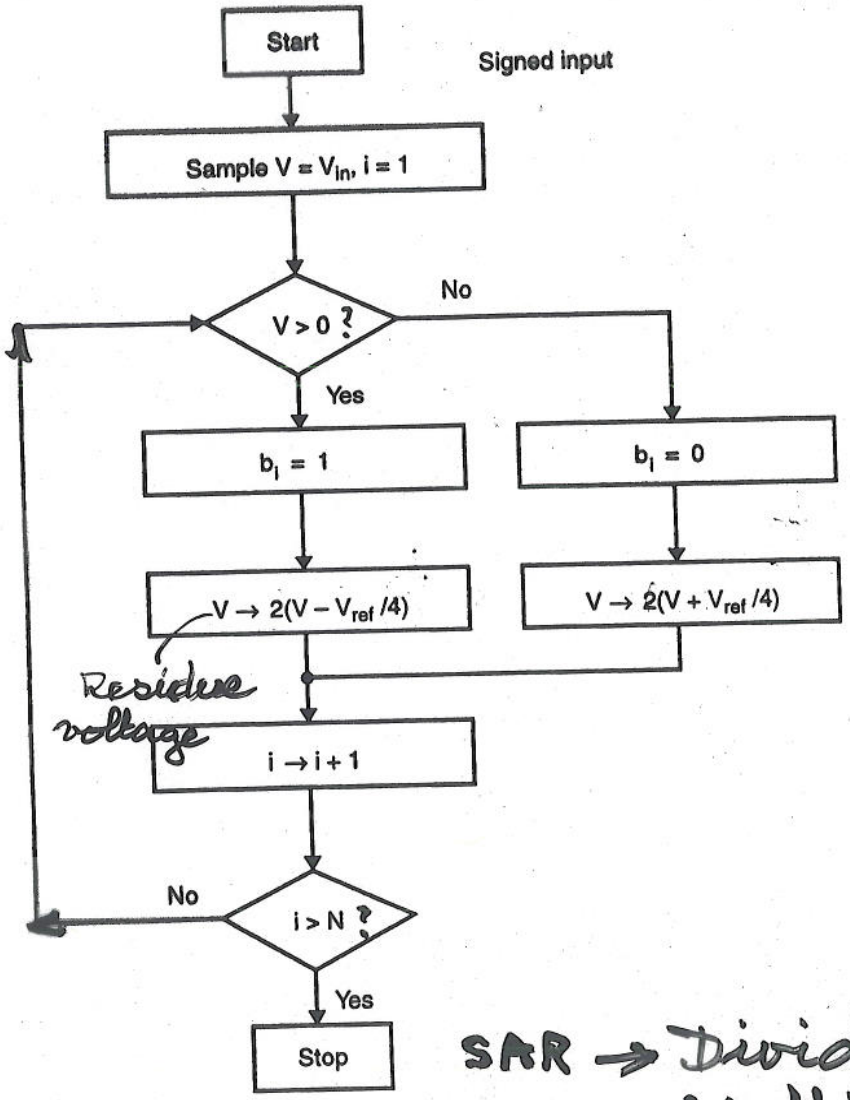
2. Multiplied remainder algorithm:

$2V_{err} = 2(V_{in} - V_r/4) \overset{?}{\geq} V_r/4$

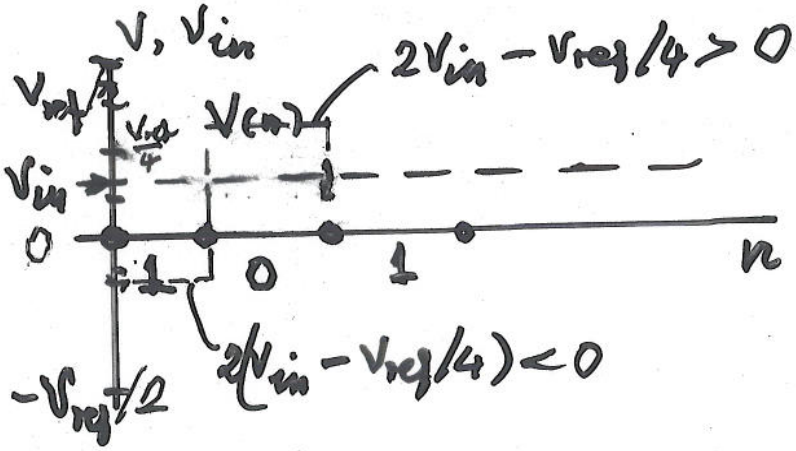
Same answer! ("No")

Serial, multiplied remainder.

Algorithmic (or Cyclic) A/D Converter (Bipolar)



- Operates similar to successive-approx converter
- Successive-approx halves ref voltage each cycle
- Algorithmic doubles error each cycle (leaving ref voltage unchanged)

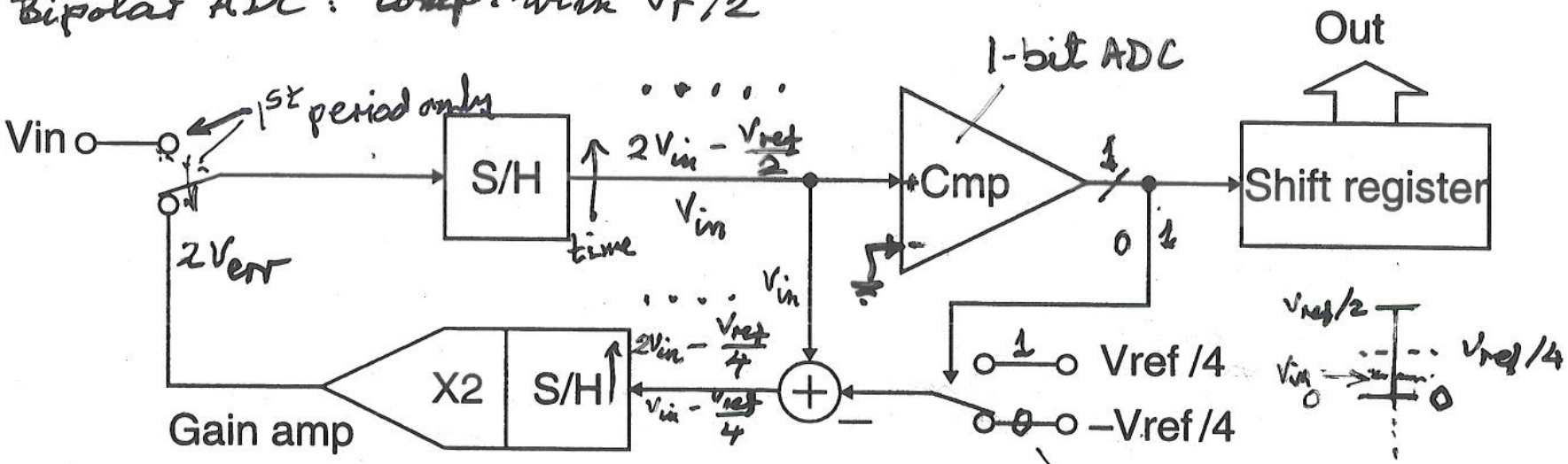


SAR → Divided reference
Algo. → Multiplied remainder

University of Toronto

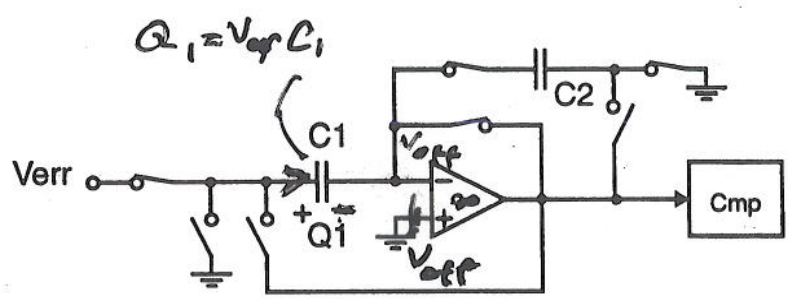
Ratio-Independent "Algorithmic" Converter

Bipolar ADC : comp. with $V_r/2$

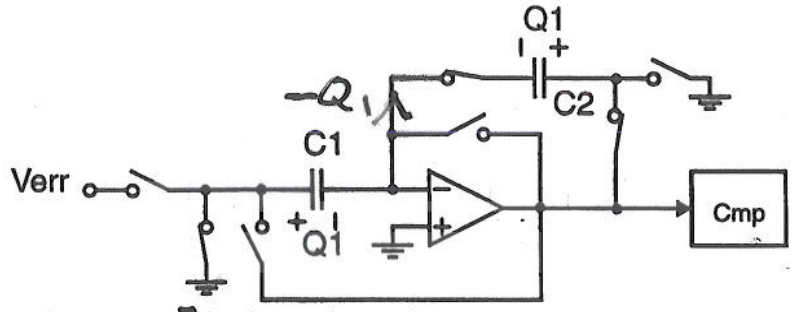


- multiplied remainder method
- McCharles, 77; Li, 84
- Small amount of circuitry (SC circuit) — reuse cyclically in time
- Requires a high-precision multiply-by-2 gain stage
- Basis of commonly used pipeline ADC

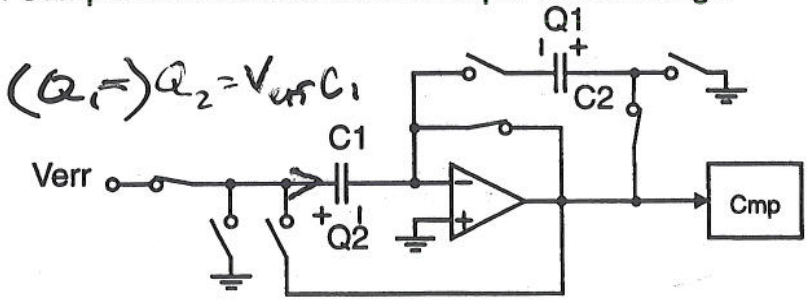
Ratio-Independent Algorithmic Converter



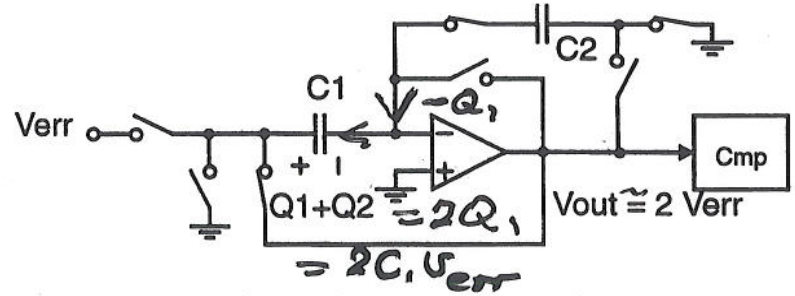
1. Sample remainder and cancel input-offset voltage.



2. Transfer charge Q_1 from C_1 to C_2.

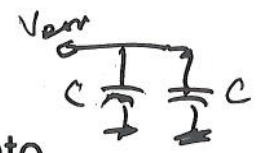


3. Sample input signal with C_1 again after storing charge Q_1 on C_2.



4. Combine Q_1 and Q_2 on C_1, and connect C_1 to output.

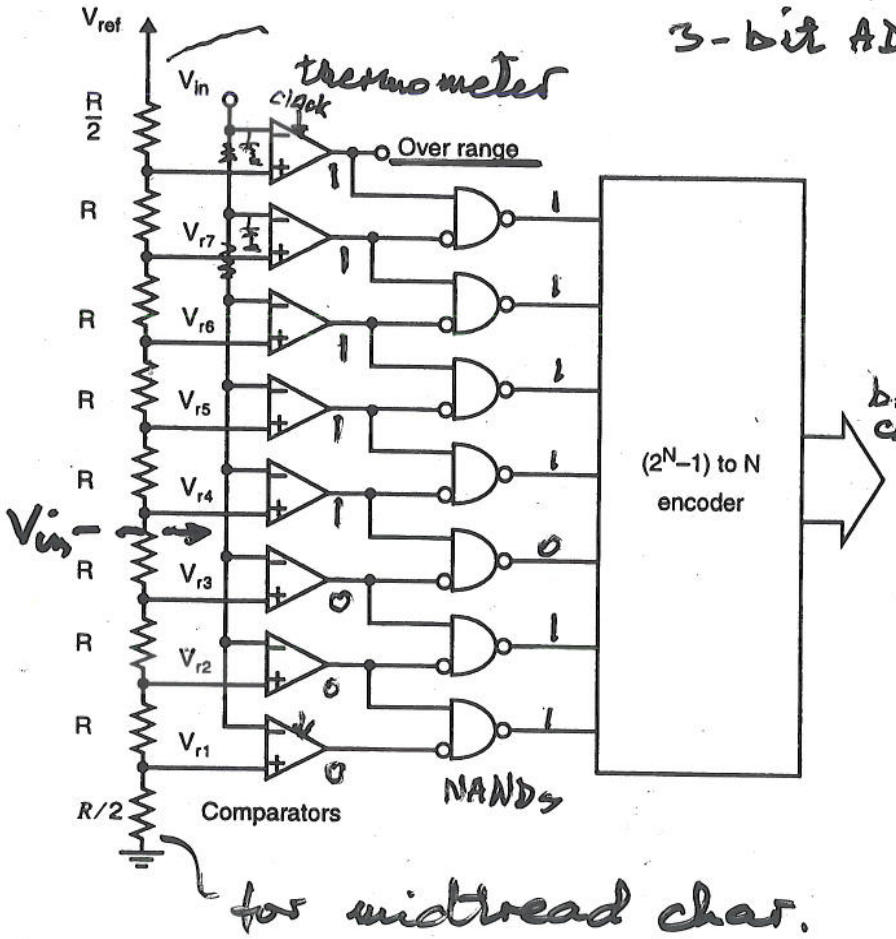
- Needs 4 phases
- Does not rely on cap matching, insensitive to V_{off}. $C_2 \sim C_1$
- Sample input twice using C_1; hold first charge in C_2 and re-combine with first charge on C_1



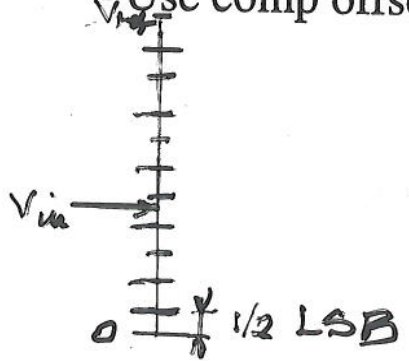
simpler, but ratio dependent.

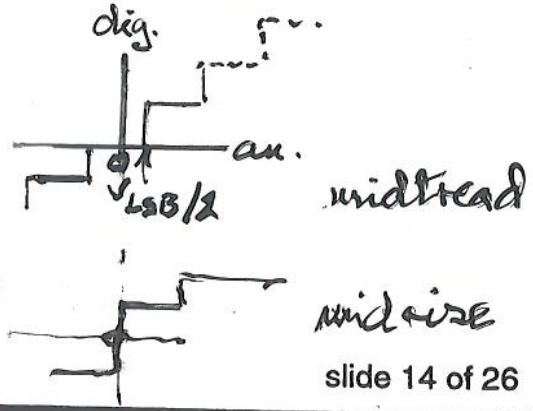
Flash (or Parallel) Converters

- Peetz, 86; Yoshii, 87; Hotta, 87; and Gendai, 91



- High-speed ADC
- Large size and power hungry
- 2^N comparators, Rs, NANDs, ...
- Speed bottleneck usually large cap load at input (comp.'s C_{in}).
- Thermometer code out of comps (sometimes better — $\Delta\Sigma$ ADC!)
- Nands used for simpler decoding and/or bubble error correction
- Use comp offset cancellation CDS





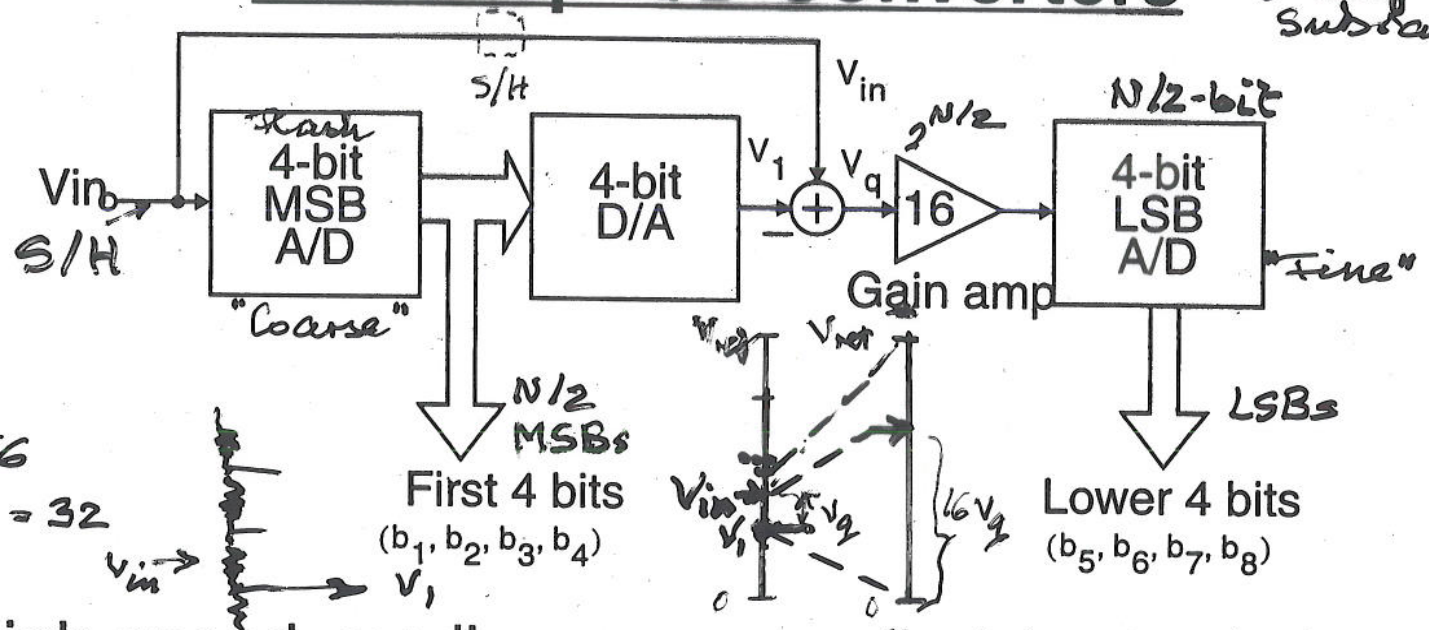
Video-freq. ADC

8-bit Two-Step A/D Converters (Half-Flash)

Subranging

$2^4 = 16$

$2^8 - 1 = 255$



Complexity

$2^8 = 256$

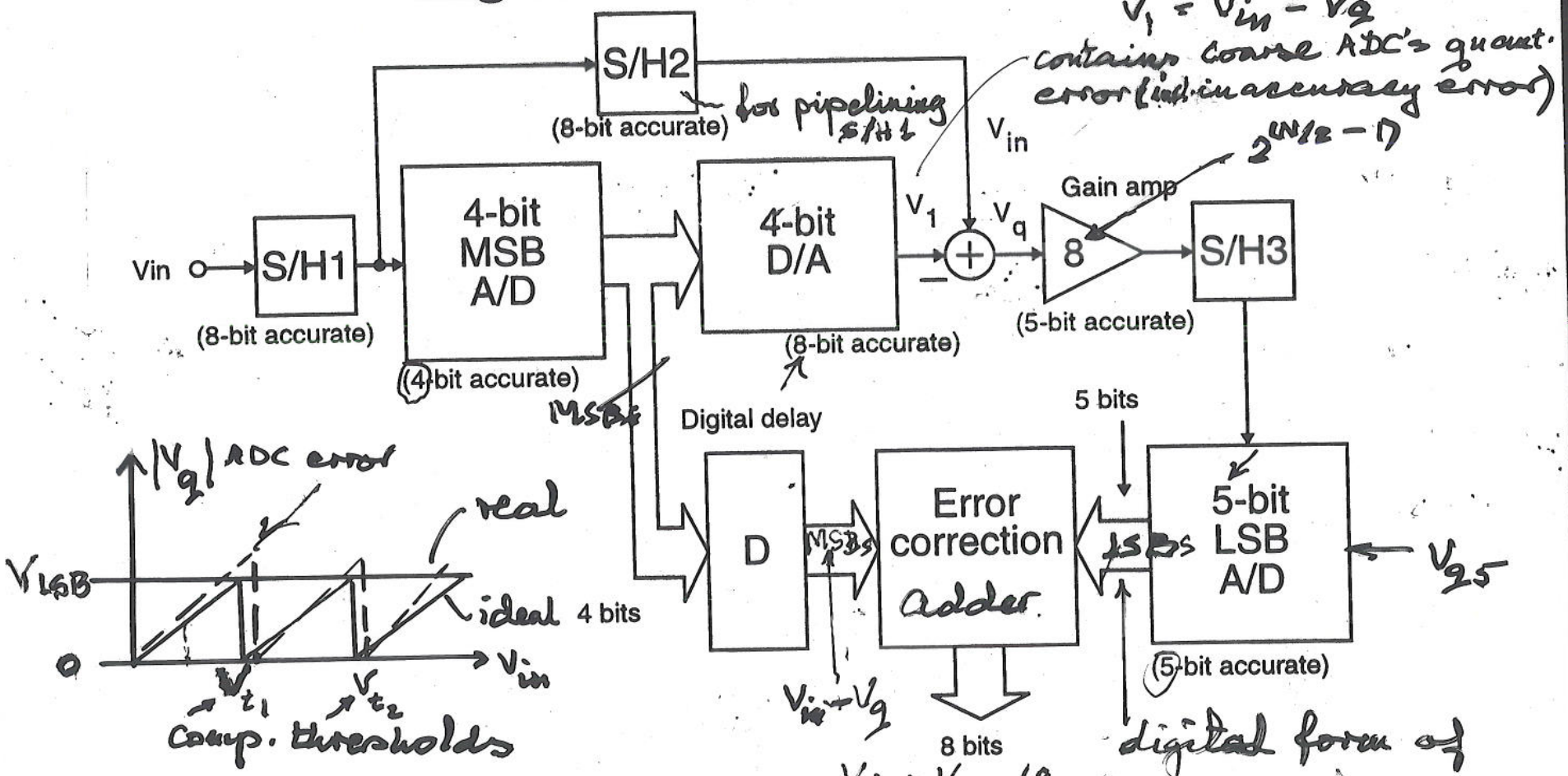
vs. $2^4 + 2^4 = 32$

- High-speed, medium accuracy (but 1 sample latency)
- Less area and power than flash
- Only 32 comparators in above 8-bit two-step (256 before)
- Gain amp likely sets speed limit (16 if reused)
- Without digital error correction, many blocks need at least 8-bit accuracy (9)

Here, 2T conv. time

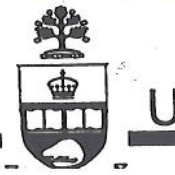
(MSB ADC, DAC, ×16 ampl., S/H)

Digital Error Correction



- Relaxes requirements on input A/D
- Requires a 5-bit 2nd stage since V_q increased
- Example, see [Petschacher, 1990].

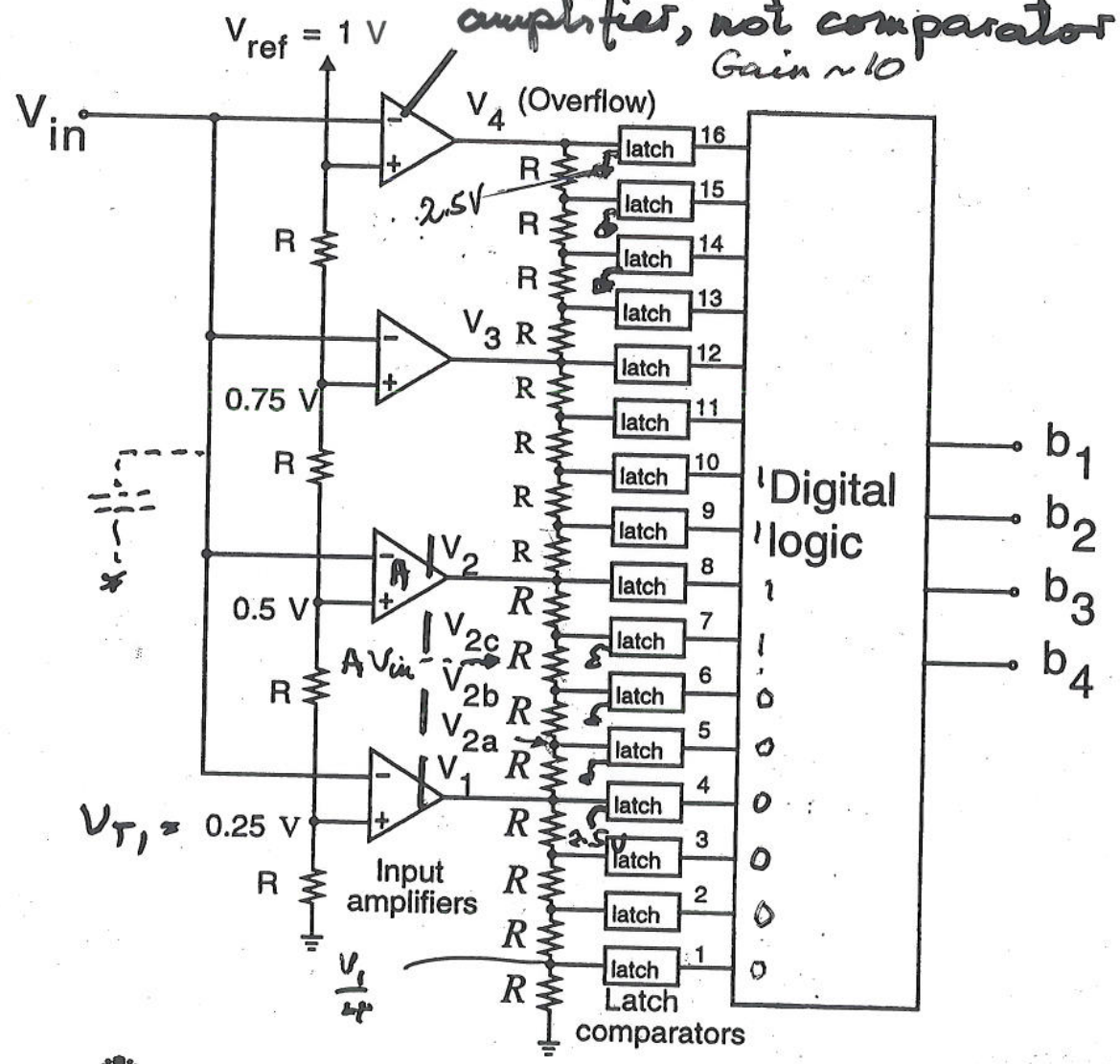
3 bits
MSBs
LSBs



4 bits.

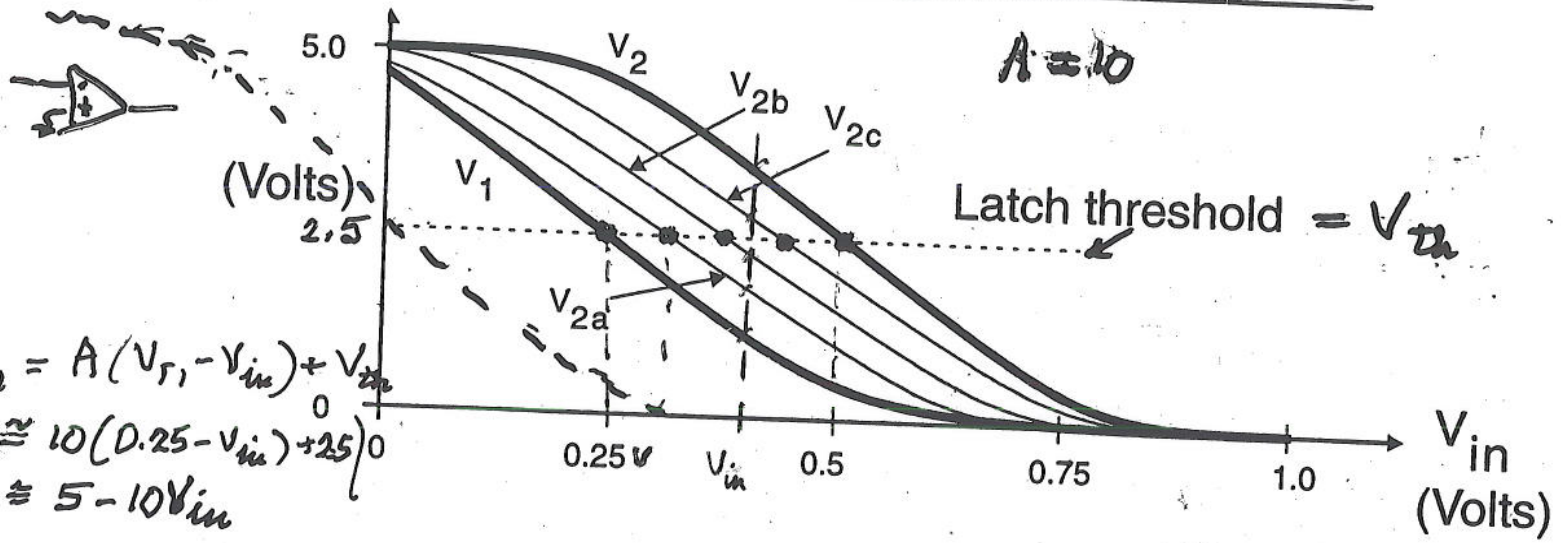
$2^N \rightarrow 2^{N-2}$ preamps

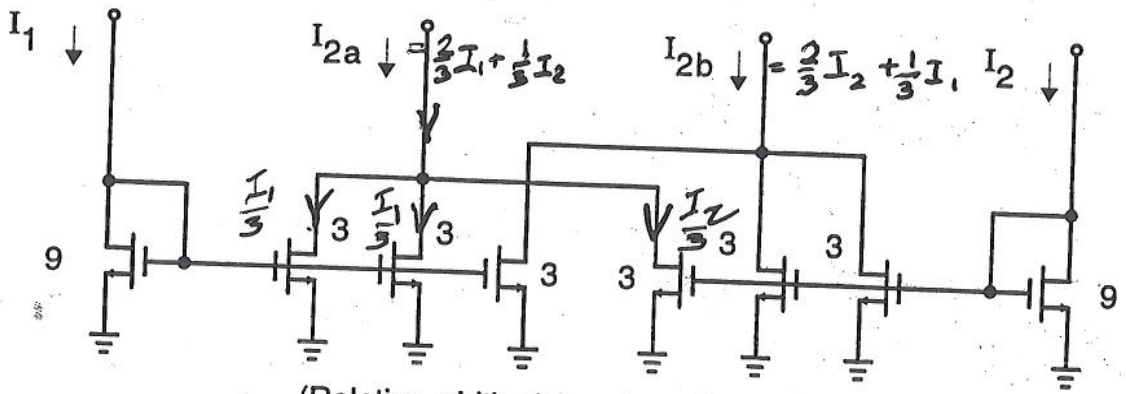
Interpolating A/D Converters



- Goodenough, 1989
- Steyaert, 1993
- Kusumoto, 1993
- Use input amps to amplify input around $2^{N/2}$ reference voltages
- Latch thresholds less critical (V_{in} is amplified before latch)
- Less cap on input (faster than flash)
- Match delays to latches
- Often combined with folding architecture

Interpolating Converters





(Relative width sizing shown)
(All lengths same)

current interpolation