Serial/Pipelined DACs

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Outline

• Serial 2C DAC
  – Operation

• Capacitor Mismatch and Mismatch Compensation
  – Capacitor mismatch
  – Mismatch compensating switching
  – Spectrum shaping
  – Radix-based digital correction

• Two-Capacitor DAC Enhancements
  – Time interleaved 2-C DACs

• Pipelined quasi-passive cyclic DAC
  – Operation
Quasi-Passive Cyclic DAC

• Operation:
  – Charge redistribution between two equal-valued capacitors
  – Serial digital input; LSB first
  – $\Phi_1$ and $\Phi_2$ are two non-overlapping clock phases
  – Conversion follows equation

$$V_{out} = V_{ref} \sum_{i=1}^{N} b_i 2^{-i}$$

Capacitor Mismatch

- Capacitor mismatch effects
  - Conversion accuracy limited by capacitor matching
  - Capacitor mismatch introduces nonlinearity
  - Plots show performance degradation (bottom) in SNDR and SFDR compared with output spectrum from DAC with ideal matching (top)
Mismatch Compensation (1)

• Switching techniques
  – Compensative switching
    • The roles of the two capacitor is interchangeable
    • The roles of the capacitors can be chosen on bit-wise base
    • An algorithm was developed to minimize the conversion error for any digital word
    • The switching pattern is input dependent
    • First-order error canceled for 31% of the input codes; reduced to 1/10 for 48% of the input codes

Mismatch Compensation (2)

- Switching techniques
  - Complementary switching
    - Digital word fed to 2-C DAC twice; once with normal arrangement, once with swapped roles of \( C_1 \) and \( C_2 \)
    - Output sof the two conversions are added (or averaged)
    - First-order mismatch compensated at cost of doubled conversion time

Mismatch Compensation (3)

- **Switching techniques**
  - Input-word-splitting compensative switching
    - Compensative switching [2] does not compensate for all input codes
    - Split digital input into sum of two digital codes
    - The conversion errors need to be able to be respectively compensated using compensative switching for the two new digital inputs
    - Final output is the sum of the two conversions

- Needs two sets of 2-C DACs
- Needs analog summation
- Needs sophisticated algorithm for splitting the input word

Mismatch Compensation (4)

• Switching techniques
  – Alternately complementary switching
    • Roles of $C_1$ and $C_2$ are swapped alternately in the first cycle and adopt complementary switching [3] for the second conversion cycle
    • Output of the two conversions are summed (or averaged)
  
  • INL improved due to cancellation of major second-order error

  – Hybrid switching
    • Averaging conversion results of complementary switching and alternately complementary switching
    • Smaller INL; fourfold conversion cycles

Mismatch Compensation (5)

• Mismatch shaping
  – Using oversampling $\Delta \Sigma$ Modulator
    • Digital state machine to control switching sequence of a symmetric two-capacitor DAC
    • Improved linearity; better shaping for higher OSR
    • Needs $2N$ clock cycles for $N$-bit D/A


Simulated (FFT) performance of the DAC without (a) and with (b) mismatch shaping using a second-order loop filter
Mismatch Compensation (6)

- Radix-Based Digital Correction
  - Compensation in digital domain
    - Effectively a radix-\((C_1/C_2)\) conversion
      \[ V_{out} = V_{ref} \left( \frac{C_1}{C_2} \right) \sum_{i=1}^{N} b_i \left( 1 + \frac{C_1}{C_2} \right)^{-i} \]
    - Assumes known mismatch \(2(C_1-C_2)/(C_1+C_2)\), or \(C_1/C_2\)
    - ADC-like algorithm predistorts digital input
    - Feeds predistorted digital words into the 2-C DAC
  - Better performance when DAC resolution is high
  - Need to find mismatch with high accuracy

DAC output spectra plots for (a) uncompensated condition, (b) alternately complementary switching, (c) radix-based algorithm and (d) radix-based algorithm with one extra bit.
Two-Capacitor DAC Variations

- **Time interleaved 2-C DAC**
  - Time interleaving 2-C blocks improves throughput speed
  - Capacitor mismatch among channels tolerable
  - Direct-charge-transfer buffer reduces power consumption

- **Pipelined quasi-passive cyclic DAC**
  - Same operation as 2-C DAC
  - Information passed on to the last capacitor and DCT output buffer

Pipelined Quasi-passive DAC

Pipelined Quasi-passive DAC

Fig. 2. System block diagram of 10-bit D/A converter.
Pipelined Quasi-passive DAC

Fig. 3. The mth stage of the converter.

Fig. 4. Unit cell of a CMOS implementation.

Fig. 7. Differential nonlinearity response.
Pipelined Quasi-passive DAC

I. CAPACITOR MISMATCHING
   SOLUTION:
   LARGE UNIT CAPACITORS
   CAREFUL LAYOUT

II. NONZERO SWITCH ON–RESISTANCE
    SOLUTION:
    LARGE TRANSISTOR SIZE

III. CLOCK FEEDTHROUGH CHARGES
     NO EFFECT ON LINEARITY (gain & offset errors only).
     Dummy switches reduce charge injection.

IV. Capacitive coupling btw. $C_i$ & $C_{i+1}$: guard strips help.

V. Last switch must be "on" when output is sampled.

VI. Buffer must be $N+1$-bit linear to avoid charge injection from last switch.
References on Quasi-passive DAC


