CS 271 Computer Architecture and Assembly Language

Self-Check for Lecture #2

Solutions

1. Terms / Definitions
   a. “caching” is moving information from slower storage to faster storage, where it can be accessed more quickly.
   b. A “bus” is a set of parallel "wires" for transferring a set of electrical signals simultaneously.
   c. "von Neumann architecture" refers to computer architectures that store programs in memory, and execute them under the control of the instruction execution cycle.

2. Inside the computer, machine instructions, memory addresses, numbers, characters, etc., are all represented as electrical signals.

3. In the simple CISC architecture discussed in Lecture, which register holds
   a. the current machine instruction? The Instruction Register (IR).
   b. the current micro-instruction? The Control Register.

4. Number the order of steps in the instruction execution cycle.
   ___ 3 ___ Decode the instruction in the Instruction Register.
   ___ 4 ___ If the instruction requires memory access, determine the memory address, and fetch the operand from memory into a CPU register, or send the operand from a CPU register to memory.
   ___ 2 ___ Increment the Instruction Pointer to point to next instruction.
   ___ 5 ___ Execute the instruction.
   ___ 1 ___ Fetch the instruction at the address in the Instruction Pointer into the Instruction Register.
   ___ 6 ___ Repeat from step 1.

5. Consider the virtual machine levels in the diagram at the right. At each level (except 0 and 5), an interpreter accepts an instruction from the level above, converts the instruction to its own language, and passes the resulting instructions to the level below. Note that Level-0 has no interpreter; the instructions from the Microarchitecture level are sent directly to the hardware.

Suppose that the interpreters at each level (levels 1 - 4) generate n instructions in order to represent one instruction from the level above. Suppose also that each Level-0 instruction executes in c nanoseconds.

   a. How long does it take to execute a Level-3 instruction? __cn^2__ ns.
Going from level-3 to level-2 creates n instructions. For each of those n instructions, going from level-2 to level-1 creates n instructions, so there will be \( n^2 \) micro-instructions, each of which requires c nano-seconds to execute.

b. How long does it take to execute a Level-5 instruction? __ cn^4__ ns.

6. How many bits in 35 MiB? \(35 \times 2^{20}\) (Bytes) x 8 (bits per Byte) = 293601280 bits

Questions 7-10 refer to the IA-32 architecture discussed in Lecture.

7. What is the width of the internal bus? __ 32 bits __

8. What is the size of the general-purpose registers? __ 32 bits __

9. Which of the following are valid 8-bit register references?

- YES  AL refers to the 8 low-order bits of EAX
- YES  DH refers to the 8 high-order bits of the 16 low-order bits of EDX
- NO    SH not allowed. This would be ambiguous, because we have ESP, ESI, and SS registers.
- NO    EL can’t divide the ES register

10. Why does protected mode prevent programs from changing the EIP register directly?

The EIP contains the memory address of the next instruction to be fetched. Since the programmer ordinarily will not know the absolute address where any of the instructions are stored, protected mode restricts access to EIP, and allows it to be changed only by the operating system.

11. True / False:

a. TRUE A MASM program must have a procedure named “main”.

b. TRUE END main is a directive that tells the operating system where to begin execution of the program.